Status of Trigger Server electronics

**Topics:**
- Trigger Server Status
- TSS screening
- TSM and SB pre-production tests
- LVDS Jitter tolerance measures
**Trigger Server – Status update**

**TSS (1200 ASIC, Alcatel 0.5 µm):**
- full production already delivered
- currently: screening of 1200 working devices ready to start

**TSM (250 TSMS + 500 TSMD pASIC, Actel, 0.35 µm):**
- 1000 device (to be fused) in hands
- Final Prototype successfully tested!
- 1 month to fuse all chips
  (ext firm already contacted): wait for pre-production tests of the Server Board (End Apr.)

**Server Board:**
- pre-production delivered in March. 03 (5 SB)
- 2 SB successfully tested!
- Pre-series production will start soon (beginning of May) -> to provide 35 SB for '03 minicrate production
- tender for full production going on
Screening will be performed in Bologna with the test jig setup for prototypes.

- **Piggy board** mounted on a **Pattern unit** emulating Traco input and receiving output.

- **TSS Asic**
  - Alcatel 0.5 µm CMOS
  - Product by Europractice
SW developed in Visual C++, fully automatic

*) interfaces Power supply and clock generator through GPIB protocol

*) interfaces mySQL database for bookeeping

Full test:
- Bonding check
- Running test (different conf, Clock frequency and Voltage supply)
- Monitor and control logic check (Jtag and Parallel access)
- Spying and Test features (snap and test reg.s)
- Power consumption continuously monitored
Performances of the test system:

- **Bonding check** (< 1 s)
- **Test sorting in different setups with 10^6 patterns** (~16 s @ 60 Kevt/s)
- **Test monitoring and control logic** (~ 5 s)
- **Bookeeping into the database**

Delivery consists of 2700 chips

- Process yield 70%
- Package yield 90% (conservative estimate)

To have 1200 TSS working
We need to test ~ 2000 chip

2 min/chip

4 weeks!

With a working time of 4 hour/day
Reminder: TSM is implemented with 3 pASIC Actel A54SX32 0.35 μm CMOS

NB: Backside contains most of the control logic electronics for the minicrate
Developed under WinNT with Visual C++

SW controls all test options:
- Generates, transmits and receives pattern
- Checks output with emulation
- Finds better setup conditions
- Provides monitoring and configuring

SW to use for full SB production test.
TSM design – a reminder…

TSM system is the bottleneck of the trigger electronics on chamber. It is segmented on 3 pASICs with partially redundant functionalities:

Two main working modes:
- **Normal mode** (all pASICS work properly)
- **Backup mode** (one or two pASICS in failure)
TSM algorithm – another reminder..

Remember: TRACO sends 2 tracks belonging to the same trigger events in 2 consecutive BXs

**TS task**: to sort two best tracks in two consecutive BXs

**Normal mode**: implemented by sorting 1 track out of 6 for BX  
**Backup mode**: each half chamber sorts 2 tracks independently in two BXs, by means of a “quick” sorting (quality bits are involved)

**Main features** (enabled in default, can be switched off):  
- Recovery of “good” track eventually found at the previous BX (called *carry*)  
- Ghost rejection  
- Recovery of “good” tracks in overlapped events (i.e. pile-up between tracks from events in consecutive BXs)
Server Board Tests Summary (2 boards fully tested):
- Board layout was checked and approved for production.
- Signals transmission from Pattern Units has been successfully checked!
  (N.B: it has the same characteristics of transmission from Trigger Boards)
- TSM monitoring and configuring works fine!
- TSM output tests with LVDS transmission through 40 m cables has been performed.

TSM Algorithm Tests Summary:
- First test: About 1000 “surgical” input patterns have been initially used.
  These “surgical” patterns, developed during the chip design and simulation, 
  thoroughly check all functionalities, in different configurations also.
- Second test: About $10^9$ random input patterns have been submitted with different 
  configurations in long tests periods (3-4 days) to find bugs and check stability and performances

Results:
- TSM and SB work as expected up to 44 MHz of clock frequency and transmitting output through cables long up to 40 m.
LVDS Trigger Link

- Opto-Link
- Sector Collector Board
- Balcony
- Sector Collector VME Crate
- DTTF (in USC55)

"Ethernet" cables
(up to ~40m)
CLASS 6 FTP
Z₀ = 100 Ω

MB 1
MB 2
MB 3
MB 4
Jitter Measurements

Jitter Tolerance measured in Bologna
- Stand-alone LVDS transmission system equipped as the final trigger link system
- Clock Jitter generator
Maximum Jitter tolerated from *National* Serializer LVDS in worst conditions with Cable of 40 m lengths
=> RMS = 80 ps

Jitter Tolerance measured in Legnaro
- TTCex driven by TTCvi
- TTCoc inserted
  (Optical input power = -20dBm)
- TTCrx in MC sends clock on LVDS ser.
- No Broadcast command
- Measured : RMS = 26 ps