DT Trigger (primitives & muon sorter)

- Minicrate: in production
- Sector Collector: prototypes
- Wedge Sorter: production finished
- Barrel Sorter: proto almost ready

- 12x Wedge Sorter
  In: max 12 tracks from 6 f Track-Finder of a wedge
  Out: 2 "best" tracks

- 1x Barrel Sorter
  In: max 24 tracks from 12 Wedge Sorters
  Out: 4 "best" tracks
Main functionalities:
- a SC board serves a sector (4/5 stations)
- track sorting (1 out of 2 tcks/station)
- DT trigger path synchronization (compensate for Time-Of-Flight, TTC fibers and LVDS cables) via clock delay and pipe lines.

LVDS link:
- 2 Ethernet cables/minicrate FTP cat.6
- TX rate @ 480 Mbps (< 50 m), with National Semicond. chipset:
  a) serializer 10-1 DS92LV1021 (8 IC/link)
  b) cable equalizer CLC014 (8 IC/link)
  c) deserial. 1-10 DS92LV1212A (8 IC/link)

Opto link:
- 6 multimodal fibers (Ericsson)/SC (< 100 m)
- TX rate @ 1.6 Gbps, with GOL serializer (32 bits @ 40 MHz), and Honeywell opto-ICs:
  a) VCSEL trasmitter HFE4190-541
  b) Pin Diode receiver HFD3180-102
Sector Collector to Track Finder opto-link

- 1 Opto RX (4 ch) board / PHTF
- 2 Opto RX (5 ch) board / ETTF
- Opto Tx (6 ch) piggy board

LVDS Rx piggy boards

- PHTF (φ view) 6 board/wedge
- ETTF (η view) 1 board/wedge

Stratix-GX FPGA used as:
- Deserializer
- RX parity checker
- I/O Router

TF crate backplane

Same boards

MB1
MB2
MB3
MB4

Clock
Control
Vcc

F.Odorici-INFN Bologna
Tridas week, 15-Mar-05
**SC prototype-schedule (4 SC-boards for Cosmic Challenge 2005)**

<table>
<thead>
<tr>
<th>Boards</th>
<th>Design</th>
<th>Board proto</th>
<th>Test</th>
<th>End (4 boards)</th>
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<tbody>
<tr>
<td>Opto Tx piggy</td>
<td>Mar Q1</td>
<td>Mar Q4</td>
<td>Apr Q4</td>
<td>May Q2</td>
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<tr>
<td>Opto Rx board</td>
<td>Mar Q1</td>
<td>Mar Q4</td>
<td>Apr Q4</td>
<td>May Q2</td>
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<tr>
<td>LVDS Rx 4 ch piggy</td>
<td>Apr Q1</td>
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<td>LVDS Rx 2 ch piggy</td>
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<td>Mother board</td>
<td>Jul Q1</td>
<td>Jul Q4</td>
<td>Aug Q4</td>
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**SC production (2005)**

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<th>Prod End</th>
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<tr>
<td>Opto Tx piggy</td>
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<tr>
<td>Opto Rx board</td>
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<td>Mother board</td>
<td>60 (10)</td>
<td>Oct Q2</td>
<td>Dic Q4</td>
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Minicrate assembly

2 assembly sites: Padova & Bologna (gradually optimizing procedures)

Present production rate: ~ 2 minicrate/week

Up to now: 24/250 minicrates assembled
Combined test PHTF-WS

During this week Wedge Sorter (preproduction) is being tested together with more PHTFs in Vienna setup at CERN.

I/O will be tested at 40 MHz.

The WS processor is programmed with “final” algorithm.

- Emulation of inputs of n PHTF @ 40 MHz
- Read back the output through WS
- Trigger output (TTL)
  - eventually for Cosmic Challenge
Wedge Sorter production

- 1 evaluation board delivered and successfully tested with our test jig
- Full production (17 boards) finished: delivery expected for this week
- Each board will be fully tested with our test jig
Barrel Sorter requirements and design approach

**TASKS:** BS algorithm is similar to WS one BUT
- 24 input tracks $\Rightarrow$ much bigger I/O ($\sim 870$)
  $\Rightarrow$ complex ghost busting
  $\Rightarrow$ sorting 4 out of 24 (heavy task)

**Design approach** similar to WS:
- All functionalities on one big FPGA:
  - Altera StratixII EP2S130, 1508 fBGA (new device!!)
- 9U, 400 mm VME board
- Latency: 3 BX for ghost-busting + sorting&multiplexing

with some main different features:
- Inputs from cable (LVDS) through connectors on board top
- Main FPGA on mezzanine board
Barrel Sorter motherboard

Optional trigger output (NIM/TTL/ECL) ..can be used in Cosmic Challenge to send trigger to LTC

- 8 layers
- pcb ready
- 3 boards will be mounted this week
- Electrical scheme ready
- Routing will start next week
- Presumably 18 layers pcb
- Proto by end of April 05
## Milestones update

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<th>Module</th>
<th>Status</th>
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Changes into:

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Boards status file

In red, modified/new items:

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