12 WS, each one sorts the 2 “best” tracks out of max 12 tracks coming from the 6 Sector Processors of a wedge.
WS hardware location

2 Wedge Sorter 9U boards per DT Track Finder crate
WS requirements 1: ghost busting

Sector Processors (DTTF) can extrapolate two tracks using common segments: single muons can appear as dimuon events.

We aim to keep the fake rate in single muon events below 0.5%.

WS can suppress the ghost by knowing the locations of track segment used by different Sector Processors to build a complete track.
WS requirements 2: fast sorting

• 2 muon candidates per wedge to keep high efficiency on dimuon events:

  sort 2 out of 12 candidates in 2 BX

• sorting is based on track quality (3 bits) and pt (5 bits):

  8 bits per track

HEAVY COMPUTATIONAL TASK

• each output track consists of 31 bits (qual, pt, φ, address, η)

  in total about 450 I/O pins

LARGE DEVICE REQUIRED
Design approach

• Use VHDL for design development

• Minimize the usage of vendor dependent libraries:

  combinational VHDL code for sorting (about 5000 lines !!)  
generated by C++ application

• Test the same design on different vendors platforms (thanks to design portability)

• Aim to fit all the logic in one single device
Design cross-check

- Wedge Sorter working rules
- VHDL design
- SW test
- HW test

- VHDL or Gate-level Simulator
- C++ Event Generator
- C++ Device Emulator
- Output Analyzer
- Pattern Unit
- Device
- Patter Unit
## Processor technology

<table>
<thead>
<tr>
<th>Feature</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Algorithm optimization</strong></td>
<td>😊😊😊</td>
</tr>
<tr>
<td><strong>Core performance</strong></td>
<td>😊😊😊</td>
</tr>
<tr>
<td><strong>Routing dependent performance</strong></td>
<td>😊😊😊</td>
</tr>
<tr>
<td><strong>JTAG access</strong></td>
<td>😊😊😊</td>
</tr>
<tr>
<td><strong>Already used in DT regional trigger</strong></td>
<td>😊😊😊</td>
</tr>
<tr>
<td><strong>Software tool interface</strong></td>
<td>😊😊😊</td>
</tr>
<tr>
<td><strong>Software tool reliability</strong></td>
<td>😊😊😊</td>
</tr>
</tbody>
</table>

- The design fits one APEX®20KE400, 672 pins FineLine BGA
- The sorter core takes ~ 19 ns
- The max frequency is ~ 53 MHz
- ~ 25% resources used, ~ 100k equivalent logic gates
Performance of ghost busting algorithm was tested with Orca 6.2.0:

- 1000 single muons \textit{(preliminary!)}
- \(3.5 < p_t < 200\) GeV (flat distribution)
- \(-0.8 < \eta < 0.8\) (flat in barrel)
- \(0 < \phi < 2\pi\) (flat)

<table>
<thead>
<tr>
<th>Wedge Sorter ghost suppression</th>
<th>Barrel Sorter ghost suppression</th>
<th>2(\mu) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>ON</td>
<td>&lt;0.3</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>8</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>17</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>27</td>
</tr>
</tbody>
</table>

D. Bonacorsi, S. Marcellini

!!!!!!
Preliminary board geometry

Electrical schemes almost ready

- **Inputs from ETTF (84 bits)**
- **Outputs to Barrel Sorter (62 bits)**
- **VME control**
- **VME (J1)**
- **Backplane: inputs from 6 DTTFs (292 bits)**

- **Apex 20k BGA 672 pins**
- **Acex 1k**
- **LVDS drivers**
- **GTL+ tranceivers**
- **GTL+ tranceivers**

Main Processor
Board testability

JTAG access (from on-board connector or VME)

Patterns from/to 3 Pattern Units at 40 MHz (through adapters boards)
Summary

- FPGA design with Ghost buster and Sorter is completed: desired performances are achieved with one single Altera APEX 20K device

- Flexible and user-configurable track elaboration

- 2 out of 12 (8 bits words) is performed in less than 20 nsec!

- Fake rate on single muon events less than 0.3% (preliminary)

- Board electrical design is in very advanced phase...BUT some delay expected due to temporary loss of manpower (1-2 month delay w.r.t. original milestone: "WS board prototype - January 2003")

- In parallel we are starting to prepare the test jig:
  - control software for Pattern Units and JTAG chain
  - adapter boards