DT Wedge Sorter status

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- **12** VME-9U board in regional DT trigger crates in USC55
- **Fake cancellation and sorting of** tracks reconstructed by Sector Processors
- **Design based on** Programmable Devices (PLD)
**WS fake cancellation**

Fake generation: consecutive SPs can reconstruct tracks having common segments

- Fake tracks suppression: algorithm checks track's segments positions
- Algorithm tested with flat single $\mu$ sample in ORCA

% of di-$\mu$ (fakes) at trigger chain stages:

from SPs 27%  **WS**  8%  BS  0.3%  to GMT
The 2 out of 12 sorting algorithm is the speed-limiting WS task.

The WS algorithm fits a single APEX20K(E)400 (Fully parallel sorting).

Apex family was simulated to choose the specific device.

- Speed grade -2 simulated performance of 42 MHz now increased up to 49 MHz through some design & layout optimization.
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Algorithm's user configuration

- The WS chip will be interfaced to the VME controller through a JTAG and a parallel interface
- This will allow to set algorithm configuration parameters
  - Sorting rules (i.e. special conditions, noisy or dead stations, etc.)
  - Fake cancellation rules (which track of the pair to cancel)
  - Track cancellation mode
- WS PLD will include snap registers to spy/test internal functionality
WS board features

VME 9U, 400 mm depth board. Main critical issues:

- 84 GTL+ bits from ETF
- 62 LVDS bits to Barrel Sorter
- 292 GTL+ bits from 6 SPs
- WS PLD
- VME PLD
- VME j1
- LVDS drivers
- GTL+ transceivers
WS board features

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- Routing problems @ fineLineBGA
  simplified by accurate chip pinout
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- Private Jtag and parallel interfaces between VME PLD and main PLD for snap and configuration registers
WS Board design status
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• OrCAD design completed
• Netlist submitted to mastering company
  ✓ PCB layout under progress
• Prototype board delivery expected within the beginning of June
  ✓ Proto-done January 2003 milestone shifted to June 2003
• Stand alone test will start as soon as the board will be delivered
• Static bonding test
  ✓ Mastering company supplies 3D RX control
  ✓ JTAG is accessible through a on-board connector or the VME controller
• Exhaustive functionality test
  ✓ WS board tested @ 40 MHz with 5 Pattern Units
  ✓ Adapter boards for \texttt{LVTTL\rightarrow GTL+} and \texttt{LVDS\rightarrow LVTTL} conversion designed
Full test control software will be developed
- to manage VME/JTAG accesses
- to send test patterns, to read and check the WS outputs
Summary

• PLD design is completed and optimized
• Algorithms effectiveness is checked
  ✓ Fake rate reduction (down to 0.3 % with WS-BS)
  ✓ Flexible configuration of algorithms
  ✓ Optimization of the parallel 2-out-of-12 sorting
• Board design is completed, prototype is in production
  ✓ Prototype board delivery expected for the beginning of June
• Test facilities (crate, VME PC, Pattern Units ecc.) are ready in Bologna
  ✓ Stand alone test setup will start as soon as prototype WS board will be delivered