DTTF muon sorting: Wedge Sorter and Barrel Sorter

- **1 BS**, it sorts the 4 “best” tracks out of max 24 tracks coming from the 12 WS of barrel.
- **12 WS**, each one sorts the 2 “best” tracks out of max 12 tracks coming from the 6 PHTF of a wedge.
### WS and BS: hardware location

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- **Z**:
  - A: TK PS res
  - B: DAQ
  - C: DAQ
  - D: Peak. FEC
  - E: DT TbkFnd
  - F: TTC
  - G: TK. FEC
  - H: Pixel FEC

- **WS and BS**: hardware location
  - (2 WS / crate) x 6 crates
  - ~ 5 m (2 BX)
  - 1 BS / 1 crate

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Combined diagram showing hardware layout with labels indicating locations for various components.
**Wedge Sorter requirements 1: ghost busting**

PHTFs can extrapolate two tracks using common segments: single muons can appear as dimuon events.

We aim to keep the fake rate in single muon events below 1%.

WS can suppress the ghost by knowing the locations of track segment used by different PHTFs to build a complete track.
WS requirements 2: fast sorting

- 2 muon candidates per wedge to keep high efficiency on dimuon events:

  sort 2 out of 12 candidates in 2 BX

- sorting is based on track quality (3 bits) and pt (5 bits):

  8 bits per track

  HEAVY COMPUTATIONAL TASK

- each output track consists of 31 bits (qual, pt, φ, address, η)

  in total about 450 I/O pins

  LARGE DEVICE REQUIRED

Latency budget: 2 BX (as in TDR)
Design approach

- Use VHDL for design development
- Minimize the usage of vendor dependent libraries
- Test the same design on different vendors platforms (thanks to design portability)
- Aim to fit all the logic in one single device

- The design fits one APEX©20K400, 672 pins FineLine BGA
- The sorter core takes ~ 21 ns
- The max frequency is ~ 48 MHz
- ~ 25% resources used, ~ 100k equivalent logic gates
Design cross-check

Wedge Sorter working rules

VHDL design

SW test

HW test

VHDL or Gate-level Simulator

C++ Event Generator

C++ Device Emulator

Output Analyzer

Pattern Unit

Device

Patter Unit
Wedge Sorter: prototype board layout

VME 9U, 400 mm depth, 10 layers

Input from ETTF (84 bits)

Output to BS (62 LVDS pairs)

Clock buffer & delay line

LVDS drivers

GTL+ transceivers

Main FPGA

VME interface

JTAG

Switching regulators

1.5V

2.5V

5.0V

3.3V

GTL+ transceivers

Input from PHTFs (292 bits)
WS design features

Main FPGA (672 pin FineLine BGA) pinout fixed before VHDL compilation in order to simplify board routing

Series termination foreseen for all data and clock lines

3 possible clock sources, with phase adjust from VME

JTAG chain through FPGA and configuration device: access from connector or VME

Ad hoc parallel interface + private JTAG serial line between Main FPGA and VME: access from VME to internal configuration registers, snap registers, test registers.

Ghost busting and sorting algorithms are fully configurable in order to adapt to different working conditions (noise, dead stations, etc).
WS: adapter boards for testing

Shielded flat cables

TTL

GTL+

LVDSTTL

128 bits I/O
up to 100 MHz

Pattern Unit

VME

TTL

TTL

GTL+

LVDS

WS: adapter boards for testing

A.Montanari-INFN Bologna

ESR for DTTF system, Vienna 19-Apr-2004
VME pattern generator and readout @ 40 MHz (Pattern Unit)

TTL to GTL adapter board

LVDS to TTL adapter board

VME flexible extender

TTL to GTL adapter board

10 m twisted pair cable
WS: standalone static tests

Tuning of switching regulators: no noise on board

Test JTAG chain: program VME interface and main FPGA (as a simple multiplexer)

Access VME chip with I/O operations

Inject static signals on GTL+ inputs by using Pattern Units and adapters boards and read back the output from the board: check of BGA soldering (first board had ~15 unconnected pins!)
WS: standalone dynamic tests

Check data and clock signals after long path on the board and tune series resistors

Inject signals @ 40 MHz, multiplex them in main FPGA, read back the output after 10 m of LVDS cable transmission: BER < 1x10^{-12}

Inject signals @ 40 MHz and check cross-talk among lines: no effect

Ready for combined test with PHTF and ETTF
The v1.0 prototype works better than expected!

We can proceed to the production of (12 boards + spares) with no modification.

Budget 2004 (44 kCHF + 9.3 kCHF) is adequate.

Tender by summer: production done Dec 04 (as scheduled)
Barrel Sorter: requirements and design approach

Barrel Sorter requirements are similar as in Wedge Sorter

**BUT**

the I/O is much bigger (868 bits)
as the computational load (ghost busting + sorting 4 out of 24)

Same approach as used in WS:
- all functionality in one big FPGA (Altera Stratix EP1S60, 1508-pin BGA)
- 9U, 400 mm VME board
- main FPGA on mezzanine
- 24 I/O connectors (KEL type) on board

**Latency budget:** 2 BX (link from WS) + 3 BX (processing) + 3 BX (link to GMT..if >7m)
(as in TDR + 1 !!)
BS: board layout design
BS: prototype and production plans

Electrical schemes presently in design phase

VHDL for main FPGA under development

VHDL for VME interface + control from WS

First prototype expected in Nov 04

Budget 2004 for prototype (16 kCHF) is adequate

“Production” (1 + 2 spares) after tests: Mar 05

Budget 2005 for production (16 kCHF + 7.8 kCHF) is adequate
Summary

Wedge Sorter:
- standalone full test of the v1.0 prototype is OK
- ready for combined test with PHTF and ETTF
- if combined test will be positive, ready to start the production

Barrel Sorter:
- use experience gained with WS
- design underway
- expect first proto next autumn

Manpower:
2 Physicists, 1 PhD, 1 technician: 2.5 FTE