Selection of two best muon candidates in one chamber and ghost suppression

Parallel architecture

Two stage processing

Trigger Server: TSS, TSM, Server Board

TSS (1200 ASICs)

TSM (250 TSMS + 500 TSMD pASICs)

Server Board (250 pcb)
TSS: chip layout and technology

Alcatel, CMOS 0.5 μm, 3.3 V
20000 gates
208 pins
Power consumption: ~300 mW

Selection of 2 best candidates from 4 TRACOs
Ghost suppression
Fully configurable
Control access through JTAG and Parallel Interface
Spying through snap registers
Stand alone internal test features
Documentation: CMS IN 2002/011
TSS: design and test philosophy

- TSS working rules and specs
  - VHDL design
  - SW test
  - HW test

Event Generator

- VHDL simulator
  - Gate-level sim.
  - post-layout sim.

C++ Device Emulator

Pattern Unit
  - Device
  - Pattern Unit

Output Analyzer
TSS: test system

SW controls all test options:

- Provides monitoring and configuring
- Generates, transmits and receives patterns (billions of random patterns!!)
- Checks output with emulation

VME pattern generator and readout up to 100 MHz (Pattern Unit)
TSS: production and screening

~2700 packaged chips not tested delivered in 2002

Tested in house ~1300 chips with a yield of 92%
(we need 1140 + 15% spares)

Test bonding through JTAG
Test sorting:
  in different configurations up to 50 MHz
  +/- 10% Vcc
(100k patterns/configuration)
Test access through Parallel Interface
Test Snap/Test registers
  ....all chip functionalities

2 min/chip
TSS: radiation tolerance

Irradiation at: Cyclotron Research Center (CRC), Universite Catholic de Louvain (UCL), Louvain-la-Neuve, Belgium with 59 MeV protons

Flux: $3 \times 10^8$ protons/(cm$^2$·s)
Total dose: 380 krad over 6 chips
256 FFs monitored at 150 kHz

TID effects:
stable up to 30 krad (10 LHC years: 0.02 krad)

SEU (six observed):
MTBF > 3.3 LHC years (90% c.l.)
**TSM: architecture (redundancy)**

- **Controls to/from 6 TBs:**
  - TSS data from 6 phi TBs

- **TSS data from 6 phi TBs**

- **Selected TRACO data from 3 phi TBs**

- **TSMS**
  - Select bus

- **TSMD**
  - Data from 3 phi TBs
  - Theta TB data
  - Controls to/from 6 TBs

- **LVDS**
  - Data transmission to Sector Collector

**Backup mode:**
- If TSMS fails, TSMDs perform sorting on quality bits (full efficiency for single muon and dimuon pairs at Track Finder level)
- If one TSMD fails, only half chamber is lost

**Selection of 2 best candidates from up to 6 TSS**

**Ghost suppression**

**Bottleneck for both trigger and data path**
TSM: system design

TSMS and 2 TSMD are 3 distinct ICs:

- independent power lines
- in case of chip failure each I/O line can be disconnected
- two independent ways for monitoring and configuring:
  1. Local JTAG
  2. Parallel access bus with ad hoc protocol (*Parallel Interface*)

**Example of redundancy:**
local JTAG chain
TSM: radiation tolerance

TSM technology: Actel programmable ASICs (model A54SX32-3; package PQ208)

Irradiation at: Cycloctron Research Center (CRC), Universite Catholic de Louvain (UCL), Louvain-la-Neuve, Belgium with protons 59 MeV

Total dose: 4 pASICs irradiated up to 40 krad/chip (1 of them up to 70 krad) (total fluence $1.4 \times 10^{12}$ protons/cm$^2$)

450 bits monitored/chip: only 1 SEU !!

MTBF > 4.6 LHC years (90% c.l)
Server Board: layout

Top side: Server Board

Bottom side: part of Control Board

16 layers PCB

Absorbed current:
- ~600 mA on 3.3 V
- ~600 mA on 5.0 V

Control access through JTAG and Parallel Interface

TSMS  TSMD

TSMS  TSMD

9.5 cm

20.6 cm
Server Board: test setup

- **Vme board with CPU Pentium II**
- **Adapter Board**
- **Trigger Link Rx**
- **Pattern Units** (pattern generator and readout module)

**Connections and Specifications:**
- Rs232 PC serial port
- 232 bits @ 40 MHz
- LVDS link – data serialized @ 480 MHz
- 80 bits @ 40 MHz
- 2 copper cables FTP class 6 – 40 m
Server Board: test results

TSM and SB work as expected up to 44 MHz of clock frequency and transmitting output through cables long up to 40 m (test of Trigger Link, see F. Odorici talk)
Server Board: production

TSM:

TSM functionality tested with “surgical” and random pattern (10⁹)

3x250 pASIC Actel 0.35 micron delivered and fused after design validation

SB:

Pre-production of 5 delivered in March 03:
   successfully tested and design validated

1 SB installed in the minicrate and tested in May 03 test beam:
   valid integration test (see R.Travaglini talk)

Pre-series production of 35 SB delivered last September:
   to be used for 2003 minicrate production
   and tuning of burn-in procedures

Tender for full production finished:
   50 boards will be delivered spring 2004
   200 boards in autumn 2004
   all boards will be tested with our test system in house
Burn-in procedures

TSS:

done on Trigger Board (F. Dal Corso talk)

Server Board:

all components are commercial

MIL-STD883 (method 1015, 5004) procedures suggests 60 degrees for 15 days:
eliminate infant mortality without affecting
the lifetime of the components

test in bunches of 40 boards, powered and clocked

evaluate and calibrate the procedure on first bunch