DT Muon Sorter

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1xBarrel Sorter
In: max 24 tracks from 12 Wedge Sorters
Out: 4 “best” tracks

12xWedge Sorter
In: max 12 tracks from 6 f Track-Finder of a wedge
Out: 2 “best” tracks
Wedge Sorter: test and production

WS board already had a hw integration test with PHTFs and ETTF in Vienna setup @ CERN (March05)

- ✓ 3 PHTFs + WS: sorting @ 40 MHz OK
- ✓ 1 PHTF + ETTF + WS: sorting @ 40 MHz OK

Full production (12 boards + 6 spares) finished !!
(All boards fully tested with dynamic patterns with our test jig: all boards OK with full functionality)
Barrel Sorter Motherboard
Barrel Sorter Mezzanine

Ghost Busting

Sorter 1
Sorter 2
Sorter 3
Sorter 4

MUXs

75 ns

40 MHz register
80 MHz register

L. Guiducci - INFN Bologna
Barrel Sorter main features

- Ghost busting, sort 4 out of 24, 3 BX overall latency
- VME slave to tune clock phases and access main chip algorithm conf regs
  - Ghost buster block tuning
  - Quality filtering of muon candidates
  - Input masking
- Trigger output on LEMO (NIM/TTL/ECL through jumpers)
  - Configurable trigger condition
    - Quality/Pt thresholds, pattern matching, etc.
  - Internal triggering of spy registers (with directVME A24D16 readout)
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- Last but not least: firmware can be eventually updated (i.e., new trigger conditions) very easily thanks to good FPGA fitting capability
Barrel Sorter: test and production

Full test setup based on Pattern Units and bidirectional LVDS-TTL adapters

Production (1 board + 2 spares) finished !!!
(All boards fully tested with dynamic patterns with our test jig: all boards OK with full functionality)
WS – BS transmission test

Pattern Units
VME Crate
BS
ETTF Adapter
SCSI cables

WS
PHTF Adapter

Pattern Unit
TTL
“PHTF Adapter”
“ETTF Adapter”
TTL \(\rightarrow\) GTL+
GTL+

1 x Wedge Sorter
LVDS

1 x Barrel Sorter
LVDS
LVDS \(\rightarrow\) TTL
TTL

Pattern Unit
Firmwares

✓ WS main chip firmware with “final” algorithm frozen since March 2005
   integration test @ CERN

✓ BS main chip firmware with “final” algorithm frozen but still very
   handy if modifications are necessary

✓ Both WS and BS VME slave chips are frozen; no changes expected
Software

✓ VME R/W accesses are used to set any option of WS/BS boards
  ✓ Synchronization (WS, BS)
  ✓ Ghost busting (WS, BS)
  ✓ Track masking (WS, BS)
  ✓ Board status (WS, BS)
  ✓ Trigger condition setting (BS)
  ✓ Trigger spy data readout (BS)

✓ Software tools have been developed as a “big” C++ class while setting up the test jig - but different VME interface & OS!

✓ Next step: software integration with DTTF
Summary

✓ WS boards: production done, stand-alone tested: 12 + 6 spares
  ✓ Needed in cosmic challenge: 2
✓ BS boards: production done, stand-alone tested: 1 + 2 spares
  ✓ Needed in cosmic challenge: 1
✓ DTTF-WS connection tested @ CERN
✓ WS-BS connection tested in Bologna
✓ BS can output a trigger signal based on configurable settings (quality, geom, etc)
✓ BS is provided with a spy data pipe that can be readout directly by VME
✓ Software tools are not integration-ready; this is the next step