DT Muon Sorter – integration with DTTF

✓ First time BS inserted into DTTF crate

✓ Board Power: **OK**
✓ Clock inputs, PLLs locking: **OK**
✓ Trigger out: **OK**

✓ VME access to slave chip: **OK**
✓ VME access to main chip: **OK**
Integration setup:

- 1 x Wedge Sorter
- 1 x Barrel Sorter
- 1 x PHTF
- 1 x ETTF
- Input Boards

Diagram showing the setup with labels for the different components and connections.
WS/BS test features

- Bypass sorting on WS/BS and preselect which input tracks to output
- Generate WS/BS outputs according to predefined patterns

BS Spy features:
- 1 Spy Block for each input/output track
- Spy Blocks are 128 BX deep
- Internal or external trigger to Spy
- High speed readout:
  - VME bus accesses Spy Blocks memories directly
- Thanks to Janos who very quickly built test control for sorters!
Integration DTTF-WS-BS

1. Generate output patterns on ETTF to test ETTF→WS connection

Connection ok
Integration DTTF-WS-BS

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   Transmission ok
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3. PHTF and ETTF delivered (non-null) track data periodically (sync. check)
   
   Transmission ok
Sorters synchronization and latency

✓ Fine synchronization tuning

✓ Wedge Sorter and Barrel Sorter boards can shift main FPGA clock phases (~ 1 ns resolution)

✓ Phase changes effects checked, but full phase scans not done:
  ✓ It would be useful to understand secure phase windows and to optimize timing ($\Delta t$ (connections) < 1 BX ...)

✓ Latency budget

✓ Wedge Sorter and Barrel Sorter latencies

<table>
<thead>
<tr>
<th>Connection</th>
<th>Latency</th>
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<tbody>
<tr>
<td>PHTF $\rightarrow$ WS (backplane)</td>
<td>1 BX</td>
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<tr>
<td>WS (processing)</td>
<td>2 BX</td>
</tr>
<tr>
<td>WS $\rightarrow$ BS (cable)</td>
<td>2 BX</td>
</tr>
<tr>
<td>BS (processing)</td>
<td>3 BX</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td><strong>8 BX</strong></td>
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<th>wrt TDR</th>
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Summary

✓ HW (was stand-alone tested) ok: power and connections need NO fixes
✓ Small bugs on firmware fixed during tests:
  ✓ Positive / Negative sectors were swapped in WS-R (old crate...)
  ✓ Spy Blocks readout had holes in reserved VME address space

✓ This was the first integration: now the system is ready for:
  ✓ Larger / Full crate setup
  ✓ Tests with patterns from ORCA data
  ✓ Clock phase scans and timing optimization
  ✓ Long run tests to collect statistics, evaluate stability and give a BER limit
Backups

✓ Backup slides following
DT Muon Sorter

BOLOGNA GROUP:
*Alessandro Montanari* (Project Leader/Engineer),
*Luigi Guiducci, Marco Dallavalle, Giuliano Pellegrini* (Technicians)

1xBarrel Sorter
In: max 24 tracks from 12 Wedge Sorters
Out: 4 “best” tracks

12xWedge Sorter
In: max 12 tracks from 6 φ Track-Finder of a wedge
Out: 2 “best” tracks
**Barrel Sorter main features**

- **Ghost busting**, sort 4 out of 24, 3 BX overall latency
- **VME slave to tune clock phases and access main chip algorithm conf regs**
  - Ghost buster block tuning
  - Quality filtering of muon candidates
  - Input masking
- **Trigger output on LEMO** (NIM/TTL/ECL through jumpers)
  - **Configurable trigger condition**
    - Quality thresholds, pattern matching, etc.
- **Int/Ext triggering of spy memories**
  - 24 (IN) + 4 (OUT) Spy Units
  - Depth is 128 BXs
  - Direct VME D16 readout
    - (2 VME accesses = 1 track, 1 BX)
- **Last but not least**: firmware can be eventually updated (ie new trigger conditions) very easily thanks to good FPGA fitting capability
Barrel Sorter: test and production

Full test setup based on Pattern Units and bidirectional LVDS-TTL adapters

Production (1 board + 2 spares) finished
(All boards fully tested with dynamic patterns with our test jig: all boards OK with full functionality)
WS – BS transmission test

Pattern Units
VME Crate
BS
ETTF Adapter
SCSI cables
1 x Wedge Sorter
1 x Barrel Sorter
PHTF Adapter
WS

Pattern Unit
TTL
"PHTF Adapter"
"ETTF Adapter"
TTL \(\rightarrow\) GTL+
GTL+

1 x Wedge Sorter
LVDS
1 x Barrel Sorter
LVDS
LVDS \(\rightarrow\) TTL
TTL
Pattern Unit