Design and Test of the Track-Sorter-Slave ASIC for the CMS Drift Tube Chambers

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The Track-Sorter-Slave

- What is the TSS?
  a device installed on the CMS Drift Tube Chambers designed to analyze data at each bunch crossing; it contributes to the L1 muon trigger decision.

- Duties:
  - track quality sorter, background filter, Tx/Rx unit, etc.

- Boundary conditions:
  - 1200 pieces;
  - 90 I/O pins (40 bidir);
  - event processing within 25 ns;
  - complex functionality;
  - radiation tolerant.
TSS Functionalities

- Many base functionalities + programmability
- On/off-line monitoring
- Built-in self test and connectivity test (Boundary Scan)

FBT = First Best Track
SBT = Second Best Track

LEB 12 Sep 2001
Executive Plan

- **Working Rules:**
  Define rules which fully describe the TSS functionality

- **Design Joined Approach:**
  Design a “machine” which satisfy the Rules using two independent formalisms:
  - a logic description (VHDL);
  - a software Device Emulator (C language).

- **Software Tools Common Base:**
  Implement software tools with a common base for IC simulation and prototype/production verification
Methodology

TSS working Rules

VHDL design

Test-SW

Test-HW

Prototype testing

IC Simulation

VHDL Sim
Gate Sim
P.LayoutSim

Event generator

Device emulator

PatternUnit

DUT

PatternUnit

Output analyzer
Advantage elements

- **Mutual X-check:**
  The two independent formalisms used in the Design Joined Approach allow:
  - reciprocal verification of the design;
  - correction for “wrong” or “missing” Rules.

- **Software Device Emulator:**
  - allows to produce an exhaustive test vector set;
  - is a “certified” SW for prototype verification.
Basic Tools

- ASIC development system (Synopsys):
  - VHDL design;
  - IC Simulation (VHDL, Gate, Post Layout).
- Layout & Prototypes via Europractice (IMEC): cheap!
- Mask & small volume production via Europractice: cheap!
- Custom Test-Software: C language programs/libs
- Custom Test-Hardware:
  - Pattern Unit: VME board, 128 I/O, up to 100 MHz;
  - DUT Interface Board.
Radiation Test setup

TSS on 60 MeV protons beam
Prototypes Test System
Performances & Results

- **IC Simulation and test:**
  - Performances: CAD Hardware
    - Gen+Proc+Analyze (evt/h): ~ 10 K ~ 10 M
    - Full test (evt): ~ 1 M > 100 M

  Note: 1 sec of LHC running (40 M evt) 4 h test!

- **Radiation Tests (60 MeV protons, Louvain 2001):**
  \[ \sigma_{SEU} = 8.4 \times 10^{-15} \text{ cm}^2/\text{bit} \]
  IC fully tolerant up to 30 krad.
# TSS Project Steps

<table>
<thead>
<tr>
<th>Project steps</th>
<th>ASIC v. 1 Full time work</th>
<th>ASIC v. 2 Full time work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Define rules</td>
<td>0.1 y</td>
<td>0.1 y (add rules)</td>
</tr>
<tr>
<td>VHDL design</td>
<td>0.4 y</td>
<td>0.3 y</td>
</tr>
<tr>
<td>Device emulator</td>
<td>0.3 y</td>
<td>0.1 y</td>
</tr>
<tr>
<td>IC Simulation</td>
<td>0.2 y</td>
<td>0.3 y</td>
</tr>
<tr>
<td>Test System</td>
<td>1.2 y</td>
<td>0.1 y</td>
</tr>
<tr>
<td>Test SW</td>
<td>0.5 y</td>
<td>0.1 y</td>
</tr>
<tr>
<td>Interface board</td>
<td>0.1 y</td>
<td>0.1 y</td>
</tr>
<tr>
<td>Proto Tests</td>
<td>0.1 y</td>
<td>0.1 y (undergoing)</td>
</tr>
<tr>
<td><strong>Total R&amp;D</strong></td>
<td><strong>2.9 y</strong></td>
<td><strong>1.2 y</strong></td>
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</tbody>
</table>

NOTE: time invested for trigger simulation not considered!
Conclusions

- Track-Sorter-Slave R&D involved about 4 y manpower
- Most of the job dedicated to Test Tools (HW and SW)