Use of antifuse-FPGAs in the Track-Sorter-Master of the CMS Drift Tube Chambers

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Each muon subsystem has its own independent logic based on custom electronics.
DT On-Chamber Trigger Electronics

- Synchronous pipelined system (40 MHz)
- Processing stages organized in a logical tree structure
TSM: Track Sorter Master

TSM is the last element of the on-chamber electronics:

⇒ ROBUSTNESS

We decide to use FPGA with Antifuse technology

• It permits to implement redundancy architecture

• Commercial devices (specifications guaranteed by producers)

• Programmable logic (one time!) : flexibility in fine-tuning of the algorithms

• Fast technology

• Small sensitivity to SEU: low rate has been measured!
  (advantage over FPGA!)
Track Sorter Master Architecture

- **partitioning** on three blocks with **redundant** functionality:
  - 1 TSM Sorter (acts as a Sorter)
  - 2 TSM Data (act as MUXes)

**Partitioning:**
- in case of TSM Data failure we lose half-chamber information

**Redundancy:**
- in case of TSM Sorter failure each TSM Data performs as a sorter without losing information;
  - in this case each TSM Data look at half-chamber independently
TSM Sorter and two TSM Data are implemented as three distinct ICs

- independent power lines
- in case of chip failure, chip I/O can be disconnected
- two independent ways for monitoring and configuring:
  1. Local JTAG
  2. Parallel access bus with ad-hoc protocol
Example of redundancy: local JTAG net
The choice: Actel A54SX32!

- 0.35 μm CMOS
- 48,000 Gates
- Plastic Quad Flat Pack, 208 pins
- MTBF = 3.43 \(10^7\) hours

**Advantage:** the same pASIC device can be used for both TSM Sorter and Data!

➢ 250 TSM for the whole CMS:
   - 250 TSM Sorter
   - 500 TSM Data

Too limited production volume for developing 2 ASICs!
Full-functionality prototype

Very intensively tested with bit patterns mimicking the real data

Each specific aspect of the functionality was verified

Internal timing was studied in detail

Used chip logic resources: 85% TSMS      75% TSMD

• Some margin for later developments

✓ It fit the final dimensions of the board which have to be installed on the chamber!
Irradiation Tests

Problem: SEU impact on antifuse-FPGA

The SEU cross-section for high-energy hadrons (> 20 MeV) is almost independent of energy and particle type. The SEU rate due to low-energy and thermal neutrons is negligible.

Expected radiation environment in the CMS muon Barrel:
- Flux of E>20 MeV neutron: $1 \times 10^9$ cm$^{-2}$ per 10 years
- Total Ionizing Dose: 0.01 krad per 10 years

at the Cyclotron Research Centre (CRC) 59 MeV proton beam at the Universite Catholique de Louvain (UCL), Louvain-la-Neuve, Belgium
System test for ACTEL A54SX32

OS = Windows

Crate VME

Pattern Unit

CPU

Pentium II

Tx input data
Rx output data
Power supply

Flat cable
~ 10 cm

Twisted pair cable

~ 25 m

External area

Twisted pair cable

~ 10 cm

~ 25 m

Irradiation area

DUT Board

p @ 59 MeV

Rx input data
Tx output data

~ 1 m

~ 10 cm

OS = Windows

Crate VME

Pattern Unit

CPU

Pentium II

Tx input data
Rx output data
Power supply

Flat cable
~ 10 cm

Twisted pair cable

~ 25 m

External area

Twisted pair cable

~ 10 cm

~ 25 m

Irradiation area

DUT Board

p @ 59 MeV
pASIC C irradiation

- four pASICs irradiated up to 40 krads/board (one of them up to 70 krads)
- total fluence $1.4 \times 10^{12}$ protons/cm$^2$
Current drawing vs TID

Actel A54SX32-3PQ208 TID test
Oct. 2000

Icc (mA)

Vcc

0 1 02 03 04 05 06 07

krads

0 10 20

Vcc

chip1 3.3
chip2 3.3
chip3 3.3
chip4 3.3
chip1 5
chip2 5
chip3 5
chip4 5
SEU test results

1 SEU event !!!
• pASICs contain a 450 bits shift register, refreshed and monitored at 1 MHz.
• We observed 1 event showing that ~1/3 of the bits changed status
• No obvious correlation
• off-line analysis using Actel CAD tools
  • most probably the event interfered with the clock distribution

So, for the TSM, we have to calculate SEU rate/ chip

• then for the Actel A54SX32-3PQ208 chips tested
\[ \sigma_{SEU} < 2.9 \times 10^{12} \text{ cm}^2/\text{chip} \] 90% u.l. , for 59 MeV protons

• Following M.Huhtinen and F.Faccio (CMS COTS Workshop Nov. 1999) we calculate for the entire TSM system of 750 chips
• \[ R < 2.2 \text{ SEU/ chip in 10 LHC years} \]
Summary

• Use of the same devices for all IC in the TSM system for the whole detector: **antifuse FPGA Actel A54SX32** which allows:
  
  - Redundant architecture implementation
  - Algorithm fine-tuning until the final programming chip
  - processing time compliant with TSM requirements

  and assures:

  - negligible SEU rate ( < 2.2 events/chip for 10 LHC years)
  - Total Irradiation Dose tolerance
Antifuse-FPGA
(pASIC = programmable ASIC)

Silicon logic modules in high density array, interconnected by 3-4 metal layers.

Antifuses are amorphous silicon connection elements, embedded between the metal layers. Once programmed they form a permanent low-impedance connection.

- Commercial devices
- Timing delay
- Same type of device for TSMS and TSMDs
- Flexibility for fine-tuning of the algorithms