DT Trigger Server - status update

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TSS
TSM
Server Board
Trigger Link
- Final ASIC submitted 2\textsuperscript{nd} April 2001 via Europractice: technology Alcatel 0.5 \(\mu\text{m}\), full VHDL design;
- 40 ASIC prototypes received;
- positive test for radiation tolerance;
- full speed test in progress to get final validation;
- if everything will be ok, start production of full batch by end of the year using Small Volume Production by Europractice; delivery expected by spring 2002.
- the test of the devices will be done in Bologna using our test jig.

ON SCHEDULE
TSM status

- All the pASIC needed (900) for full system have been already delivered last April

- TSM-Sorter programming ready

- TSM-Data programming currently in simulation phase

ON SCHEDULE
The final design of the full board (merging of TSM side and Chamber-Controller side) is ready and the master (14 layers) is currently under preparation. On schedule.
Trigger link

- Links the Server Board to the Sector Collector;
- Designed with National parts: serializer DS92LV1021, equalizer CLC014, deserializer DS92LV1212A

were tested with a cable of 28 m @ 40 MHz

100 Gbit as random patterns &
100 Gbit as physical patterns

NO ERRORS!
Trigger link test setup

Pattern Units

TX

RX

28m Cable

CERN 06,07 Nov 01

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