Reminder:

- two stage system on chamber;
- 1080 Track Sorter Slave (TSS): ASIC devices;
- 250 Track Sorter Master (TSM): each of them composed by 3 pASIC chips.
TSS: ASIC prototype

- Final prototype received on 10th August:
  - CMOS 0.5 μm Alcatel (via Europractice: low cost!)
  - full JTAG control
  - built-in test features
  - reference manual almost ready (CMS internal note)

10 ceramic, 30 plastic package

~20000 gates

120 pads

4.5 mm
Test tools

40 MHz clock

91 I/O @ 40 MHz: use Pattern Unit.
hardware ready, software almost ready

DUT

JTAG access: tested ok
Test tools

Pattern Unit:
128 channels
up to 80 MHz
Irradiation tests on TSS: CRC

6 prototypes irradiated at CRC Louvain:

- 60 MeV protons
- Total fluence: $2.8 \times 10^{12}$ p/cm$^2$
- Total equivalent dose: 389 krad

Expected in Muon Barrel (in 10 years):

- >20 MeV neutron fluence: $1.0 \times 10^9$ n/cm$^2$
- Total dose: 0.01 krad
Irradiation tests on TSS: TID

TID test on TSS (Alcatel 0.5 μm)

No effect up to 30 krad!
Irradiation tests on TSS: SEE

<table>
<thead>
<tr>
<th>Chip</th>
<th>Dose (krad)</th>
<th>#SEE (&lt;30krad)</th>
<th>#SEE (&gt;30krad)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C10</td>
<td>70</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>C9</td>
<td>84</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>C5</td>
<td>98</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>C6</td>
<td>98</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>C1</td>
<td>19.6</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>C2</td>
<td>19.6</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Chain of 256 FFs monitored through JTAG circuitry

Six SEE after 386 krad

$$\sigma_{SEU} = 2.3 \times 10^{-15} \text{ cm}^2/\text{bit}$$

More events after 30 krad threshold..!?!
TSS production

• Irradiation test was ok (through JTAG)
• still to be completed the test at 40 MHz

• ready to start production and test of 1500 pieces at the end of 2001
• we will use Small Volume Production with Europractice (reduced cost mask set);
• the test of chips will be done at home.

We are on schedule with milestones:

<table>
<thead>
<tr>
<th>DT</th>
<th>TSS ASIC</th>
<th>Production start</th>
<th>Dec-01</th>
</tr>
</thead>
<tbody>
<tr>
<td>DT</td>
<td>TSS ASIC</td>
<td>Begin Delivery</td>
<td>Jan-02</td>
</tr>
<tr>
<td>DT</td>
<td>TSS ASIC</td>
<td>Production done</td>
<td>Apr-02</td>
</tr>
</tbody>
</table>
Track Sorter Master (pASIC)

On schedule with milestones:

- Received 900 chips from Actel
- TSMS programming ready
- TSMD in simulation phase: programming test in Nov 2001
- Server Board (TSM side) electrical schemes ready: wait for integration test with Controller components to be placed on the other side.

On schedule with milestones:

<table>
<thead>
<tr>
<th></th>
<th>TSMS, TSMD, PASICs</th>
<th>Production start</th>
<th>Jul-01</th>
</tr>
</thead>
<tbody>
<tr>
<td>DT</td>
<td></td>
<td>Begin Delivery</td>
<td>Jan-02</td>
</tr>
<tr>
<td>DT</td>
<td></td>
<td>End Delivery</td>
<td>Apr-02</td>
</tr>
</tbody>
</table>

25-Sep-01

A.Montanari, INFN Bologna
LVDS trigger link test

@ 30 MHz: $3 \times 10^{-11}$ errors/bit
@ 40 MHz: $1 \times 10^{-9}$ errors/bit
Irradiation tests on Trigger Links

Devices irradiated up to 80-90 krad without damages

SEE under study..but seems negligible:

2.4x10^-9 errors/bit @ 40 MHz

Preliminary