Proposal of a readout technique for low-pitch pixel devices

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Abstract
The up-to-date radiation position pixel detectors designed and constructed for high-energy physics, as Large Hadron Collider experiments at CERN, share comparable on-chip readout electronics. They implement full-custom 2D matrices of sensitive elements, which are basically readout via token-based techniques, according to trigger signals. As the readout phase is one of the crucial points of large matrix devices, here it is described a novel readout architecture of pixel devices, which exploits the features of the state-of-the-art deep-submicron CMOS technologies and could be applied to low-pitch pixel circuits. This allows for future applications not only to general pixel detectors but also to trackers and trigger systems, wherever an on-line data reduction is required.

Conclusions
The solution can be easily investigated and designed suing and exploiting the state-of-the-art CAD tools (digital synthesis, place-and-route, etc.). Moreover, the approach might be associated with a custom-designed matrix to a final mixed-mode ASIC design. The wiring complexity is independent of the number of pixels as these are no point-to-point wires; all the lines are global. The proposed approach could match the requirements of future low-pitch pixel detectors that need robust on-chip digital sparsification and that may also be used as first level triggers in trackers or vertex detectors.

The readout steps are carried out until all the hits are read.

At a given time the hit situation is shown in Fig. 1.

Description of an example
Let’s give a brief functional description by following the Fig. 1-7.

At a given time the hit situation is shown in Fig. 1.
Five hits are present and, consequently, 3 OR_r and 3 OR_c wires are high thanks to the wired-or condition.

Now, only the most-left column that contains at least one hit is enabled. All the other columns are masked via the RES_c lines. Fig. 3 shows this situation and the OR_r lines indicate which pixels on the selected column have hits and which have not.

Then this column can be reset via RES_c and RES_r combinations and 2 hits are reset at the same time. Fig. 4 shows this reset phase.

Then the process moves to the right and the same steps are carried out until all the hits are read.