Development and test of a front-end electronic board for the NEMO Km³ telescope

The telescope NEMO Km³

The NEMO collaboration is involved in a research for a huge deep underwater Cherenkov light detector for neutrino astronomy. A Km² scale telescope would be able to detect some events per year for neutrinos with energies above 10¹⁶ eV.

The method of detection was proposed by M.A. Markov in the early 60's. The charged current interaction of a neutrino with a hadron generates a relativistic mean which can emit Cherenkov light if propagating in a transparent medium like water or air.

The light is revealed by thousands of optical modules equipped with photo-multiplier tubes and read out electronics. A three dimensional structure, consisting of a square grid of towers, sustain all the OMs spread over a volume of 1 Km³.

Digital samples of each photo-electron signal are sent to the shore station by an optical fiber. The arrival time on each PMT, and the relative position, is the information used to implement a first level trigger.

The Optical Module and the front-end board

The board was designed to realize both a versatile prototype for simple debug operations, but also a fully functional and specification-compliant board. This prototype integrates the analog front-end LIRA and an FPGA, a reconfigurable digital control logic device for pre-processing, storing and transmission. The communication system has been realized according to the transmission protocol used in NEMO Phase-1.

The interface towards the PMT integrates a signal conditioning circuit made up of decoupling transformers and 100MHz low pass anti-aliasing filters.

The chip LIRA is socketed giving the chance to test more chips on the same board and is powered by independent linear voltage regulators. External trimmers allow the fine adjustment of voltage settings for the acquisition pedestals and thresholds.

The trigger device starts the acquisition of photo-electrons and waveforms in the switched capacitor arrays. Each output of the delay line is multiplexed towards a fast pipelined ADC counting 25MS/s.

The whole digital logic of the board is supplied by an FPGA, a Xilinx Spartan 3E 250 Kigates, which leads the acquisition process, stores the digital samples and controls the communication with the next data concentrator.

For debug purposes, two detachable debug modules were added. They integrate a led display, a temperature sensor, a quartz oscillator and two push buttons and a switches. This solution allows to save a considerable area on the main board and to remove all the light-emitting electronics foreseeing a test with a real PMT in a dark room.

The analog Acquisition

The front-end board is based on the full custom ASIC called LIRA (“analog delay line” from the Italian acronym) for PMT's waveforms analog sampling.

Two parallel delay lines sample both the anode and the dynode pulse increasing the linear dynamic range. The sampling rate is 200 MHz. A third channel is used to sample at 200MS/s the 20MHz square-wave main clock to retrieve the fine temporal information of a pulse start with a resolution of 1ns. An off-line sample interpolation can bring out a precision of 1ns.

Two identical blocks of this three-channel memory, are available in the full custom LIRA chip. They compare the anode signal to different voltage thresholds: it triggers the acquisition process when the lower threshold is crossed and thus classifies the pulse dynamic range with a higher threshold. A time threshold is also used to distinguish between a narrow single photo-e. pulse, a close double shot or a complex over-threshold waveform.

Nemo Phase I and NEMO Coincidence

The collaboration has monitored different kind of environmental parameters, such as water optical properties and currents intensity, in many sites of the Trrirreno and Ionian sea. Mainly two sites have been pointed out, one for a test apparatus (Phase 1), and one for the eventual definitive design.

The test apparatus called Nemo Phase 1 has already been realized and it has been deployed few Kms away from the coast of Catania in December 2006. This prototype was made up of a single tower housing 16 OMs distributed on 4 floors. The onshore station is situated in the harbor area of Catania.

Now a later testing apparatus called Nemo Phase 2 is under research. It will be made up of a higher tower, 16 floors and 64 OMs, to be deployed in one of the optimal sites: 100 Kms away the coast of Capo Passero.

Two of these floors will be dedicated to new R&D projects about the front-end acquisition system, following the technology improvements and exploring new acquisition strategies. The remainder, up to now, will be equipped by the same technology adopted in NEMO Phase-1. The experimental board described here wants to study a different front-end philosophy. A more evolved solution, descending from this idea, will be deployed in one of the R&D floors of NEMO Phase-2.

The first power-on test has shown an overall correct working. The system gave good results. (PLL, temp. sensor...)

A specific test was dedicated to the communication system towards the nearest data concentrator. For these purposes a communication test bench has been set up using all the hardware components actually present on the NEMO phase-1 concerning data transmission. With it has been possible to receive samples on a PC and to send commands towards the DAQ Board itself.

A particular test was designed to verify the secure flexibility to the board framework without introducing any other device but a PROM and a MUX. Thanks to this solution it is possible to upgrade on line the FPGA firmware and to grant a backup solution on the primary ROM.

The Analog Acquisition

This front-end solution is based on the full custom ASIC called LIRA (“analog delay line” from the Italian acronym) for PMT's waveforms analog sampling. The technology used is 0.35 µm, and the working principle is a set of switched capacitor.

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The optical module at NEMO, a versatile prototype for simple debug operations, but also a fully functional and specification-compliant board.

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