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Abstract
This work is aimed at defining the architecture of a new digital ASIC, namely Slow Control Architecture (SCA), which will be designed and fabricated in a commercial 130 nm CMOS technology. This chip will be embedded within a high-speed data acquisition optical link (GBT) to control and monitor the front-end electronics – post-processing electronics for front-end sensors - proposed for future high-energy physics experiments at the super-Large Hadron Collider (SLHC), CERN, Geneva. The GBT link provides a transparent transport layer between the SCA and control electronics in the counting room. It will be provided with rad-hard redundant logic for critical circuits. The project follows a set of designs that were recently developed via a 250 nm CMOS technology for LHC experiments. Since this 250 nm specific technology used to design ASICs for the LHC will no longer be available as it was in the past, requesting an update technology for future experiments must be satisfied in any case. A test chip that implements three different redundant methodologies against Single Event Effects is also described. The ongoing work is within the Italian DACEL2 collaboration.

1. Introduction
The Gigabit Bi-directional Trigger [1] (GBT) and the Slow Control Architecture (SCA) designs are special purpose integrated circuits that will be developed, fabricated and distributed in a commercial deep-submicron 130 nm CMOS technology. It is proposed to implement a control link system in the future SLHC trackers [2] to control and monitor the embedded front-end detectors and sensors. This paper presents the main features of the entire optical link along with the motivations that guided the technological and architectural choices. It describes in detail only the SCA design, which is mostly oriented to slow-control operations. In addition, the entire link organization is not only limited to applications in a single tracker, since no special features and/or constraints of the tracker have determined its architecture. Hence, it can also be adapted to any experiment at SLHC.

The SCA design is under development and some of its features might be changed to better fulfill the requirements of all the experiments. In addition, some features might be enhanced.

It should be noted that the link architecture described in the paper is not only composed of custom devices designed via CMOS VLSI technologies but it is also a structure that will be classified as a rad-hard optical link for the specific environment foreseen for SLHC. For example, it requires a further effort to choose an appropriate methodology, while designing digital ASICs, to stand the radiation-induced effects. In more detail, the electronics has to stand the total ionizing dose (TID) and the single event effects (SEE). For the TID, several studies were done in the past: it has been found that a commercial 130 nm technology is intrinsically radiation tolerant for the expected TID at SLHC [3,4]. Conversely, for the SEE each ASIC requires its redundant logic. Hence, it has been decided to use commercial standard cells as basic digital elements to design digital circuits as they are expected to stand TID effects. In this work, we have investigated three different common SEE redundant solutions to select the more suitable for the SLHC environment.

The above work of characterization against a harsh radiation environment was done in the past to characterize the 250 nm rad-hard technology used to design many chips. Now, these ASICs are implemented in many front-end detectors of the LHC experiments. However, as the 250 nm technology node was not sufficiently radiation tolerant against TID, a set of non-commercial standard cells was designed from scratch to implement dedicated layout structures against TID – the library development took years [5, 6]. This is why this technology cannot be easily replaced by other 250 nm technologies available on the market and hence, it has been decided to move toward a deeper technology node such as the 130 nm that now can be found at a reasonable cost, while providing self-tolerant components against TID.

Figure 1 shows a two-chip architecture for the data acquisition chain and for the slow-control from the front-end detectors to the counting room. In particular, the architecture uses two fibers that share data acquisition streams, timing and trigger signals and provide the slow-
control. The slow-control link between GBT and SCA implements an Ethernet protocol. In this way, the user will be able to interface the optical link with his electronics. The same Ethernet protocol is also used to pack data to and from the counting room via optical fibers. The GBT will be a rad-hard chip and have a custom transceiver to interface with the optical fibers.

The right hand side of Fig. 1 shows the slow-control Ethernet bus interfacing with a commercial field programmable gate-array (FPGA). In fact, in counting room, the utilization of a complex rad-hard device such as the GBT is not justified.

The Ethernet protocol allows users to easily connect the front-end detectors to standard personal computers for testing purposes as shown in Fig. 2. This facility does not require the full implementation of the optical link, while permitting to test the front-end detectors via the slow-control chip SCA. The system requires a more in-depth and real test; the GBT chip along with its optical fibers will replace the personal computer used in laboratory. This is clearly independently of the experiment.

The communication between GBT and SCA is bi-directional and organized within packets and frames: a frame is associated to a command identifier and each command opens a transaction. Frames from GBT to SCA are called forward-frames while the reply-frames go backwards from SCA to GBT. Moreover, a queuing system for the command identifiers permits the detection of lost packets or other synchronization failures.

2. The protocol

The communication structure used by the SCA is based on two layers. The first layer connects to the GBT with standard personal computers for testing purposes as shown in Fig. 2. This facility does not require the full implementation of the optical link, while permitting to test the front-end detectors via the slow-control chip SCA. The system requires a more in-depth and real test; the GBT chip along with its optical fibers will replace the personal computer used in laboratory. This is clearly independently of the experiment.

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Figure 3 shows the proposed scheme for the SCA. All modules interface with the NC via an internal bus (Wishbone [6]). The NC is the master that allows transactions from the Ethernet port of the Media Access Controller (MAC) toward the PCs. There are 32 peripherals that use the most common slow-control protocols such as I2C, JTAG, serial, parallel and 1-wire. In addition, the MAC controller interfaces with the NC through another standard bus (Atlantic Interface [7]). In this case, the MAC is the master and NC the slave.

2.1. The SCA blocks

The SCA architecture is basically composed of the following blocks:

- MAC Controller,
- Network Controller, (NC)
- Peripheral Controllers (PCs).

The MAC Controller provides the clock, a series of handshake signals for the NC and receives commands from the counting room, via the GBT chip as shown in Fig. 1.

The NC forms the reply commands to be sent to the counting room. The NC interfaces with the PCs through common commands. In other words, the different peripherals “talk” to the NC independently of their physical layer. For example, JTAG, parallel and I2C peripherals interface with the NC through equivalent I/O ports and through equivalent commands. If a new type of PC will be required in the future, this will have to adhere
to the same bus interfacing signals as the other PCs do. In this way the system might be easily scaled to larger numbers of PCs.

An asynchronous reset at system boot to force the system into its default state is provided in addition to the synchronous reset commands for the ports.

3. Radiation Tolerance

Many methodologies have been studied in the past to design rad-hard electronics, particularly to stand the SEE via redundant logic. These solutions require in any case larger silicon area and increase the total power consumption. To limit these drawbacks, it has been decided not to apply the redundancies to entire circuits but only to a subset of critical logic like control logic, sequential blocks and registers. It can be said that registers, flip-flops and memories are the best candidates to be hardened via redundant logic.

Hence, to operate in the future SLHC tracker environments, the SCA will also be provided with rad-tolerant redundant circuits on critical logic blocks against SEE.

The measurements of leakage current on commercial 130nm standard-cells designed from linear transistors rather than enclosed-gate-transistors, have found that it is not necessary to re-design from scratch a dedicated library of standard cells against TID [7]. Conversely, redundant structures are required to protect the SCA from Single Event Upsets (SEU) and Single Event Transients (SET) [8]. These are the reasons behind exploiting different redundant architectures of a test prototype to compare robustness, power consumption, dimensions and circuit implementation complexity. In particular, three different redundant architectures have been chosen: Triple Module Redundancy (TMR) [9, 10], Triple Time Redundancy (TTR) [11] and Hamming code [12]. All these three methods correct SEU and make SET ineffective in real-time. In addition, this prototype contains a shift-register that accumulates all the detected SEU. Then, the occurred SEU can be monitored off-line and compared to those effectively corrected in real-time – i.e. not seen as errors while clocking the chip –.

The TMR architecture is often used to harden digital logic against SEE and SET. It is a well-known tolerant technique to avoid errors in complex circuits. Basically, it consists of three identical logic blocks performing the same task with concurrent outputs being compared through majority voters (see Fig. 4). The majority voters block the effects of a SEE through the logic at the final output and hence, the voters are located at the end of the combinatorial and sequential logic blocks. The drawback of this solution is the area and power consumption, which increases with the increase in number of components.

Another method, the so-called TTR architecture, handles the time evolution of the signal inside the circuit (see Fig. 5). Time redundancy is also employed to provide the advantage of redundancy as described above in TMR. Here the circuit is not tripled. In fact, the combinatorial logic output is sampled three times, via three clock phases and then the three stored outputs are compared. When a SEE causes, for example, a short glitch at the combinatorial logic output, only one of the three registers might be modified by this error. Three matching results indicate the absence of an error, while in the event of a SEE a voting circuit selects the correct result.

TTR consumes less power and area than TMR as the redundant circuit is slightly more complicated than the
original one: the number of components is also slightly increased. However, TTR requires a more complicated clock routing on the layout. In fact, the three clock trees must have a very low skew. In addition, the combinatorial time must be much smaller than the clock period available for the not redundant logic. Moreover, the three-phase structure has to easily fit (in time) within the clock period. This limits the field of applications to not very high-speed systems.

Hamming codes can also correct SET and SEU using a “parity” control. This allows the correction of single bit errors such as those generated by SEE. Hamming code method is simple but slower than the previous methods. This circuit occupies a reasonable large silicon area having a complexity comparable with the functional blocks that will be implemented in the SCA. In more detail, a general-purpose sequential digital circuit (finite state machine with a lot of combinatorial logic) composed of nearly 50k gates was designed by implementing the three previous methods described above. This allows future tests under radiation to really compare the bit-error-rates and to evaluate the best technique against SEE for this particular 130 nm commercial technology. The chosen methodology is to compare the behavior of the three different layout redundant logic schemes with the same circuit implemented without any kind of protection (“non-protected circuit”). The chosen method will be strongly recommended to design radiation-hard ASICs with the same technology, being located within a radiation environment as the one foreseen for SLHC.

Figure 6 shows the layout of the submitted test chip. The three diverse implementations are hardly visible as the three horizontal regions - rectangular shapes while the two couples of vertical bars are power stripes (the above cited “non-protected” circuit is spread over the entire layout). This is why the modern place-and-route CAD/CAE tools distribute all the standard cells over the available silicon area in order to balance the timing requirements – i.e. the propagation delays on the wires –, the routing congestion and the area constraints. An ionizing particle that crosses the circuit may deposit charge inside a region of the order of several cubic microns. The more randomly distributed the cells, the better the entire circuit against radiation. Here the initial circuit becomes no longer recognizable in the layout. To cope with an increase of two orders of magnitude in the foreseen radiation level of SLHC, with respect to the value expected in LHC, an intensive irradiation campaign will be performed on the ASIC, whose layout is shown if Fig. 6.

4. Future Test Plan

In the past, in order to achieve a reasonable safety margin, the 250 nm technology used today in several front-end hybrids of LHC experiments was initially tested up to a dose of several Mrad and a fluence of $1 \times 10^{15}$ 1 MeV/cm² n_{eq} even though these numbers are higher than the expectations of many experimental conditions of LHC.

Now, for application in SLHC, the front-end electronics will have to stand the highest amount of dose and fluence of the SLHC experiments. For this reason a fluence of $1 \times 10^{16}$ hadrons/cm² and a dose equivalent value up to 100 Mrad were chosen - independently - to characterize the technology [13]. High-energy protons and heavy ions will be abundantly produced during the LHC running experiments and therefore represent concerns for microelectronics. Moreover, for SLHC the radiation environment worsens.

Although some tests using pulsed laser sources [14, 15] might be done, our program is to irradiate the chip, in the spring 2009, by using a heavy ion beam to examine the digital SEU/SET error cross section versus Linear Energy Transfer (LET) as a function of frequency and error rate. We know from the experimental evidence [16] that scaling down with the technology the minimum surface LET value scales down too together with the saturated SET cross-section value. According to this we may estimate the expected maximum SET frequency for our “non-protected” test circuit. In fact, considering that the “non-protected” circuit contains a number of nodes (bits) of about 300 and assuming a priori a SET probability of $10^{-9}$ [cm²/bit], we expect a SET rate ranging from 300 Hz and $3 \times 10^{-2}$ Hz going from an high flux of $10^9$ ions/cm²×s down to $10^5$ ions/cm²×s.

Hence, the ASIC will be irradiated using many different ion sources like C, Al, Be and I, up to a maximum fluence of $10^7$ ion/cm², with a surface LET value ranging from 3 and 80 MeV×cm²/mg. Our test strategy will be based on the continuous counting of the SEE occurrences by monitoring the capacity of the three architectures under test to recover faulty events. Hence, their “hardness” can be estimated. During the tests the chip will be powered and clocked.
5. Conclusion

The GBT and SCA project is aimed at proposing a high-speed general-purpose optical link for the data acquisition chains of the front-end electronics for SLHC experiments and beyond [17]. For this reason many standard user-ports have been proposed along with an Ethernet protocol. The project is justified because embedded applications in modern large high-energy physics experiments require particular care to assure the lowest possible power consumption and the radiation tolerance, still offering the highest reliability demanded by very large particle detectors.

Within the project, the SCA chip will carry out the slow-control operations for the front-end electronics. In addition, as the SCA will be located in a radiation environment, it will include a robust design to stand SEE. This is why we are investigating three redundant solutions to protect logic from Single Event Upsets and Single Event Transients and we are exploiting different implementations to compare robustness, power consumption, dimensions and circuit complexity. Particularly, for redundant logic against SEE, a prototype chip has been designed and fabricated in a 130nm CMOS commercial technology, using standard cells only. For the time being, this technology is the one chosen for the electronics upgrade of SLHC. The technology upgrade toward a 130 nm node has been necessary as the previous 250 nm, which used a dedicated library of digital standard cells designed with enclosed layout transistors against Total Ionizing Dose, will be soon unavailable.

The ASIC prototype will be tested under radiation (proton and ion beam) to compare the three redundant methodologies. The one that will show the lowest sensitivity to SEE will be recommended for those ASICs that will operate in the SLHC radiation environment, not necessarily for slow-control purposes such as the SCA. SCA will interface with front-end electronics via common ports such as JTAG, I2C, parallel and 1-wire and, with the GBT (or a personal computer during test programs) via an Ethernet port. This will also allow testing general-purpose electronics, independently of the experiment.

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References