An on-Chip Fast Readout Sparsification for a 256-Pixel 3D Device

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Abstract—A prototype of a 3D ASIC built up of a fast readout architecture, with sparsification capabilities, which interfaces with a matrix of 256 pixels sensor, was recently submitted. The chosen technology is CMOS Chartered 130 nm as it is compatible with the Tezzaron facility to interconnect fate-to-face two silicon wafers allowing for a vertical integration structure by means of through-silicon vias. Particularly, the readout logic shares one layer of double-layer design that will be stacked at the end of the fabrication process.

I. INTRODUCTION

This work follows previous versions of matrices of pixels that were fabricated using the STM 130 nm CMOS technology, implementing several types of pixels, from 256 to 4096 Monolithic Active Pixel Sensor (MAPS), and different testing and readout capabilities [1,2,3]. These prototypes were fabricated and tested in the past years. As they embedded different pixel layout flavors, a vast amount of information and data were collected. The main prototype of the previous series, implementing 4096 pixels, was also measured on a CERN test beam on September 2008. The promising results have induced the VIPIX [4] collaboration to move toward even more challenging structures and silicon foundries.

The paper describes in detail the digital readout of a double-layer 3D project, designed in Chartered 130 nm CMOS technology [5]. The design includes a new version of the sensors still maintaining the parallel sparsification digital readout capabilities of the previous projects. In particular, the matrix and the readout logic have been developed separately and, eventually, integrated together. In addition, the matrix has been split into the two layers of the 3D design while the readout and sparsification logic has been implemented only in the bottom layer. The two layers form the matrix of 256 pixels that, along with parallel sparsification readout logic, build a 3-dimensional stacked device. Square groups of 16 pixels form a macro-pixel (MP). Each MP can be latched via single pixels, 40 by 40 mm each, and an 8-bit time-stamp is associated with the frozen condition. This fast architecture could overcome the well-known readout speed limit of big matrices. As the output port can only accept one-hit information at a time, an internal queuing system has been provided to stand local high hit-rates. The ASIC can be connected to an actual full-custom matrix of 3D sensors or to a digital matrix emulator composed of standard cells (flip-flops), for testing facilities. For both operating modes a slow-control phase is required to load the chip configuration via mask bits to select which MPs are to be read and which are not, for example in case they are too noisy or burned up. Previous versions of similar ASICs were designed and properly tested. The work is aimed at improving the design of a pixel detector with an on-chip fast sparsification system, for particle tracking, to match the requirements of vertex tracking system of future high-energy physics experiments. In fact, the implemented readout architecture can be data driven extending the flexibility of the system to applications in first level triggers on tracks in vertex detectors. Simulations and tests on previous prototypes designed and fabricated via other foundries, still using the same 130 nm technology node, prove that the readout system can easily cope with an average hit-rate up to 100 MHz/cm² if a master clock of 40 MHz is used, while maintaining an overall efficiency over 99%.

II. THE ASIC

This allowed for an in-depth investigation of the design, made up of two different approaches. In fact, the matrix of sensors has been custom-designed and simulated, then it has been described with a VHDL-Verilog model and used as a macro-cell block within a bigger digital design. The global place-and-route of the bottom layer has been also digitally designed. Fig. 1 shows the organization of this bottom layer of the entire 3D double-layer design. The layout is composed of a matrix of 256 pixels organized in 32 columns by 8 rows. Each pixel is squared and its size is 40 by 40 mm. The figure, even though shows the complete layout of the bottom layer, can be imagined as it was divided into an upper and a lower part. The matrix occupies the upper part of the figure. In particular, in this layer, the matrix area embeds only the digital interface of the pixels to the readout and sparsification logic. Conversely, the lower part of the same layout is filled up with std-cells - 13 thousand altogether - confined into some power and ground rings. This is the actual readout and sparsification logic and this is why this layer has been designed using a fully digital flow from synthesis to place and route. The layout is pad limited as at this stage of the research no area optimization has been studied. Hence, no matter the matrix to logic area ratio. Particularly, most of the border space has been left for the vertical stacking with the upper layer containing the sensors and part of analog electronics to collect the sensors’ signal. In fact, the border space on the left and right sides of the layout where some I/O pads lack will have to connect the top sensor layer of the 3D design through dedicated vias. Also along all
the 256-pixels will connect the upper layer through inter-layer vias.

III. THE MATRIX

Each MP is activated and frozen via dedicated wires while the reset and readout phases are carried out via long wires that are shared over the entire matrix. The dedicated wires may also be masked, one by one, in case they would be too noisy or “burned”, to avoid reading not-significant hits. The MPs that own at least one hit are seen via fast-or wires and frozen. In other words, when at least one pixel out of the 16 that build up a MP is on, an OR-function (fast-or) over the 16 pixels inside the MP is executed and an output signal goes high. Then, all the fast-or signals of the MPs indicate the status of the matrix. These MPs are then frozen via MPs’ dedicated wires. Thus, the readout phase can start over the activated MPs. The spatial coordinates of these MPs are associated with a time-stamp, whose registers are located outside the matrix. Then, one at a time, the columns of interest are enabled and the MPs’ output data are written on a readout bus. Once the MPs have been read out they are set free. Then the process moves to another column of MPs. The readout phase involves one column of MPs at a time and this leaves the rest of the matrix free and capable of detecting new hits. Thus, the matrix may own hits, along with their personal time-stamps, belonging to different bunch-crossings. During the readout phase the matrix is swept and all the hits belonging to a given bunch are read out, reset and set free. The process continues till all the MPs have been read out. All these capabilities have been designed into a single die composed of a large full-custom matrix of pixels that is read out via a standard-cell based digital circuit. Fig. 2 shows the organization of the entire matrix composed of 256 pixels. In more detail, there are:

- 8 macro-columns (MCs), addressed from left to right, ranging from 7 to 0,
- 8 rows of pixels, addressed from top to bottom, ranging from 7 to 0,

- 4 columns of pixels inside each MP addressed from left to right, ranging from 3 to 0.

Fig. 2 The matrix divided in MC, MR and MP

In this view, each pixel is identified via a MC, a single column inside the MC and a pixel row. By converting these coordinated in digital logic it turns out 3+2+3 bits, i.e. 8-bits altogether which exactly address 256 pixels. This is the way the addresses are sent to the readout output port.

IV. THE DIGITAL DESIGN-FLOW

Some of the tasks we have been standing while designing the bottom layer of the 3D device were the synthesis and the place-and-route of the VHDL code used to design and simulate the readout logic. These are normally carried out following a so-called design-flow. This latter involves several steps from a synthesis of a VHDL Register Transfer Level code to a final global check of the layout view. In between many intermediate steps are supposed to be executed depending on the design complexity and on the digital library provided by the silicon foundry. Some of these steps are crucial as concern the analysis of the circuit and the margins on the timing characteristics. Many parameters are also strictly dependent on the foundry as different constructors may require different parameterization of their components. Hence, the overall confidence with the ASIC performance depends also on the adopted design flow.

Unfortunately, as this research relies on a frontier research of vertical-integrated sensors, a corresponding digital design kit is not properly provided along with the digital cells. For this project the ARM [6] corporate allowed us to use the Chartered 130 nm digital cells but these were not accomplished with a secure and comprehensive manual. This is the reason while had eventually to cope with some unguided steps by following the most reasonable flow we could. In summary we have adopted the design steps shown in Fig. 3. The well-know tools by Synopsys and Cadence were used and some patches have been manually inserted. In particular some problems arose while importing the post-synthesis Verilog flat netlist into the Cadence environment, and some tools demonstrated to be not fully compatible – i.e. Design Rule Check for antennas and detail routing with Engineering Change Order -.

Nevertheless, all in all we have been able to overcome the above problems and converged to a reasonable confident design of the layout as shown in Fig. 1.
V. CONCLUSION

One of the aims of this project is to test the feasibility and reliability of 3D sensors using this technology. Then, results will lead to future improvements to design a high-density thin vertex detector with an on-chip sparsified digital readout system, for particle tracking, aimed at matching the requirements of future high-energy physics experiments. The new approach in the design of 3D devices, proposed by the VIPIX Collaboration, is very promising to develop a thin pixel system with fast readout for applications in silicon vertex trackers at future colliders as the SuperB [7] Factory.

REFERENCES