A DSP equipped digitizer for online analysis of nuclear detector signals

G. Pasquali\textsuperscript{a,*}, R. Ciaranfi\textsuperscript{b}, L. Bardelli\textsuperscript{a}, M. Bini\textsuperscript{a}, A. Boiano\textsuperscript{c}, F. Giannelli\textsuperscript{a}, A. Ordine\textsuperscript{c},
G. Poggi\textsuperscript{a}

\textsuperscript{a}INFN and Department of Physics, University of Florence, Via G.Sansone 1, Sesto Fiorentino 50019, Italy
\textsuperscript{b}INFN - Sezione di Firenze, Via G.Sansone 1, Sesto Fiorentino 50019, Italy
\textsuperscript{c}INFN - Sezione di Napoli, Via Cintia, Napoli 80126, Italy

Received 24 July 2006; received in revised form 27 September 2006; accepted 2 October 2006

Abstract

In the framework of the NUCL-EX collaboration, a DSP equipped fast digitizer has been implemented and it has now reached the production stage. Each sampling channel is implemented on a separate daughter-board to be plugged on a VME mother-board. Each channel features a 12-bit, 125 MSamples/s ADC and a Digital Signal Processor (DSP) for online analysis of detector signals. A few algorithms have been written and successfully tested on detectors of different types (scintillators, solid-state, gas-filled), implementing pulse shape discrimination, constant fraction timing, semi-Gaussian shaping, gated integration.

© 2006 Elsevier B.V. All rights reserved.

PACS: 84.30.Sk; 07.05.Hd; 07.50.Qx

Keywords: Digital sampling; Digital signal processing; Online processing; Data acquisition

1. Introduction

Six years ago the heavy ion group of INFN Florence started the design of a four-channel digitizing board prototype to study the application of digital sampling techniques to energy and time measurement and to particle identification [1–6]. The prototype allowed acquisition and storing of signals, without on-board analysis capability; signal treatment was performed off-line on a dedicated CPU, although the analysis algorithms were studied for an easy on-line implementation. In the following few years we have studied in detail the application of digital sampling techniques to nuclear detector signals. We have found that in several applications the same or better performance can be obtained from digital sampling as from standard analog methods (e.g. in energy and time measurement or in particle identification [1–5]). Moreover, using sampling, one can exploit the more detailed information achieved by recording complete signals and implement analysis methods with no analog counterpart (e.g. fast Fourier transforms, curve fitting, comparison with tabulated data, etc.).

Along with these studies and developments, in the framework of the NUCL-EX collaboration, we started a project for a fast digitizer with on-board processing capabilities. The project has now reached the production stage. The new digitizers are modular in structure, each channel being housed on a separate daughter-board plugged on a main mother-board. Up to eight sampling channels can be plugged on a single mother-board. Each channel is equipped with a 12-bit, 125 MSamples/s ADC and with a Digital Signal Processor (DSP) for on-board signal analysis. The DSP extracts the physically relevant informations from the signal before transferring data to the acquisition system for storage, thus relaxing its bandwidth and mass storage requirements. In fact, transferring complete signals to external (i.e. not on-board) CPUs or to a mass storage device can be cumbersome for the acquisition system, especially when an apparatus with many channels is involved. In our design, we maintained the possibility of transferring the full digitized sequence to the acquisition system in each event (typically we choose to...
2. General description of the system

The system was designed to be easily re-configured and upgraded. We favoured a modular design in which each channel is housed on a small (140 × 25 mm²) piggy back board, plugged on a main “mother” board (cf. Section 4).

The mother-board acts as an interface between the channels local bus, whose signals are for the greatest part those of the DSP direct memory access interface (IDMA) [11], and the acquisition readout bus, which in the present versions can be either VME or FAIR bus. The biggest advantages of such a structure are:

- Channels with different specifications (e.g. input stage characteristics, sampling rate) can be plugged on the very same mother-board provided they adhere to the local bus specifications, making their upgrading an easy task.
- Adding support for new readout buses (e.g. PCI [12]) would imply re-designing (in part) the mother-board but not the channel daughter-board.

3. The digitizer channel

The present version of the digitizing channel is shown in Fig. 1. Each channel features an input LEMO connector for detector signals and an 8 pin connector for the input of trigger signals (cf. 3.3) and the output of logic signals generated by the DSP and by the on-board comparators.

Fig. 2 shows a block diagram of a digitizing channel. Five sections can be identified: the analog input stage (programmable-gain amplifier and anti-aliasing filter), the digitizing section (ADC), the temporary storage section (FIFO memory), the processing section (DSP), and the trigger section (programmable comparators and trigger logic).

3.1. Analog input stage and AD conversion

The analog input stage polarity (positive or negative) can be selected via a dedicated jumper on the channel board. The ADC has a fixed input range of 2 V: the full range at channel input is, therefore, determined by the analog input gain. The input gain can be set by the on-board DSP to one of 255 different values, corresponding to a full range going from 130 mV (maximum gain value) to 8 V (minimum gain value), allowing the system to adapt to various detector/preamplifier configurations with no circuit changes.

The input anti-aliasing filter is a 3-pole active low-pass filter, whose configuration and behaviour have already been discussed elsewhere (see Figs. 4 and 5 in Ref. [1]). In the present design filter attenuation at 62.5 MHz, i.e. the Nyquist frequency of the digitizer, is ≈ 30 dB.

The on-board DSP also controls an electronic switch (see Fig. 2) which selects one of two possible ADC input sources, the detector signal and the time reference (TR) signal common to all channels (see Section 4). The TR is provided for timing coincidence and time of flight measurements (see Refs. [2,6]).

The digitizing section exploits a 12-bit ADC operating at 125 MSamples/s and having an effective number of bits (ENOB) of about 10.7 [13]. In experimental tests performed with the prototype described in Ref. [1] (a 12-bit, 10.8 ENOB, 100 MSamples/s digitizer) we achieved satisfactory resolutions both in timing measurements (100 ps FWHM with a Si detector [2]) and energy measurements over a wide dynamic range (about 15 PSENOB [5,14]). The prototype digitizer also featured good particle identification capabilities over a wide dynamic range (see Refs. [3,14]). Therefore, the presently...
employed ADC is an effective choice for a general purpose system.

Typical characteristics of the digitizing channels, in this first version, are:

- 12-bit sampling at 125 MSamples/s.
- For low noise demanding applications, like those involving germanium detectors, 10.5 ENOB are obtained using a fixed-gain input stage. For channels with programmable input gain (like those employed at GARFIELD) 9.7 ENOB are typical.
- 0.25 LSB differential nonlinearity.
- 0.8 LSB integral nonlinearity.

3.2. Storing and processing

The ADC output values are continuously written to a First-In-First-Out (FIFO) memory which stores up to 8192 samples (≈ 64 μs at 125 MSamples/s).

In many applications (e.g. for amplitude measurements) a good estimate of the signal baseline is mandatory [14–16]. In order to get this information, a suitable portion of the baseline preceding the particle signal must be sampled and collected. In our design, the first FIFO locations act as a circular buffer. They are continuously re-written while the channel is waiting for a trigger (see Section 3.3). The length of the circular buffer can be changed by programming the on-board programmable logic device (PLD) which is used mainly for channel’s glue logic.

When a trigger signal is received, the trigger logic (see Fig. 2) enables the FIFO memory to be filled up so that the first samples of the stored signal will always correspond to a time interval preceding the trigger (e.g. ≈ 4 μs for a 512 samples circular buffer) and can be used to calculate the current signal baseline. In Ref. [14] it has been shown that a baseline of a few μs length is usually adequate to spectroscopy-grade energy measurements.

The DSP can execute up to 80 million multiply-and-accumulate operations per second [11]. Its on-board RAM memory is large enough (192 kB) for signal storing and elaboration, thus no external memory chip is required. The DSP reads sampled data from its I/O port, connected to the FIFO, and stores them in its internal data memory. The acquisition system loads the DSP program in DSP internal memory and starts the program execution through the DSP IDMA interface. The DSP controls the channel hardware (the DACs used for gain and threshold settings, etc.), handles the validation logic of the event, performs signal analysis and prepares readout data in its internal memory.

The acquisition system can read/write data from/to the DSP internal memory asynchronously through the DSP IDMA interface during program execution, for instance to read event data or to instruct the DSP to change gain, thresholds, etc.

The acquisition system can check the status of the digitizing channel (idle, analyzing, waiting for readout) by accessing the mother-board local bus and polling a few logic signals controlled by the DSP.

3.3. Trigger

Signal storing in the FIFO and signal processing by the DSP are started by a trigger signal coming either from an external device or from one of the two on-board comparators. There are two external trigger inputs, one located on the 8 pin front connector and one located on the mother-board connector, the latter coming from the ECL input of the mother-board. The comparators thresholds are

Please cite this article as: G. Pasquali, et al., A DSP equipped digitizer for online analysis of nuclear detector signals, Nuclear Instruments and Methods in Physics Research A (2006), doi:10.1016/j.nima.2006.10.008
controlled by the DSP by means of a dedicated program-
mable digital-to-analog converter. The analog input signal
is shaped by a CR-RC filter \( \tau \approx 200 \text{ ns} \) before being sent
to the comparators, as shown in Fig. 2. Two comparator
ranges are available, both divided into 255 steps: one
comparator can go up to the ADC full range (“high
threshold” in Fig. 2), the other can be adjusted between
zero and 10% of the ADC full range (“low threshold”).
This allows a fine tuning of the channel threshold in order
to better treat low-amplitude signals. Comparators outputs
can also be picked out from the 8 pin front connector (for
instance to build a second level trigger for the experiment)
as shown in Fig. 2.

Another logic signal, common to all channels and
connected to all the DSPs, is fed to the mother-board via
one of the user-defined pins on the VME P2 connector and
it is typically employed to validate the digitized events. The
DSP program can test the level of this signal at any time
using a dedicated instruction (see Section 5).

4. The main board

A 6U VME board (shown in Fig. 3) was the simplest
choice as a first implementation of the mother-board, though other readout buses (e.g. PCI) can be implemented
without redesigning the digitizing channels, thanks to the
modular design of the system.

Actually, an alternative readout bus has already been
implemented on the same VME mother-board, the FAIR
bus developed by LASS laboratory of INFN-Sezione di
Napoli [10]. The FAIR bus exploits the user-defined part of
the VME P2 connector. It can reach a bandwidth of
180 MB/s in optimal conditions. As usual with FAIR
modules, the mother-board features a 32-bit multi-event
FIFO which is written with DSP data and buffers data for
read-out and event building [10]. The FAIR bus is
currently employed in a few experimental apparatuses
(e.g. the GARFIELD [9] apparatus). The mother-board
can be switched from VME to FAIR mode via a jumper
placed on the front panel (see Fig. 3).

The mother-board houses the interface from the readout
bus (VME or FAIR) to the “local” bus of the digitizing
channels. It also features an 8 input ECL connector for the
trigger signals of the eight sampling channels (see Section
3.3). A common TR signal can be connected to a LEMO
input connector on the mother-board (see Fig. 3) and
distributed to all the sampling channels as discussed in
Section 3.1. When the relevant part of the input signal has
been sampled, the DSP can start sampling the TR by
controlling the electronic switch shown in Fig. 2. The
sampled signal thus contains both the detector signal and
the TR signal. A numerical algorithm extracts the time
difference between the two, with a sub-nanosecond
accuracy. Since the same TR signal is distributed to all
the sampling channels, it is possible to perform timing
coincidences and time-of-flight measurements (the latter
may require the TR signal to have a definite relationship
to the nuclear collision like, e.g. the RF signal of a pulsed
beam). The basic idea of this method can be found in Ref.
[2], Section 5, while a more detailed discussion will be
presented in Ref. [6].
5. Algorithm structure

The on-board DSP is used both to control the channel hardware and to perform signal analysis. The general structure of a DSP algorithm is shown in Fig. 4. The DSP switches to an idle state after an initialization phase, performed once and for all at bootstrap time, where the DSP sets up its internal registers, channel gain and comparator thresholds, etc. Upon receiving a signal trigger (connected to the interrupt request signal IRQ0) the DSP jumps to an interrupt service routine which spends a few microseconds reading samples from the FIFO (usually corresponding to the baseline), then checks a validation signal (e.g. the general trigger of the experiment). In case of no validation, the DSP rearms the channel for a new trigger and returns to its idle state, otherwise it reads the remaining samples from the FIFO and restarts the circular buffer. The signal analysis phase follows. Since signal analysis lasts much longer than the buffer length expressed in μs, the buffer has been filled completely before a new trigger can be accepted. After the analysis step, the DSP prepares the output data in its internal memory for readout and returns to its idle state. Readout takes place through the IDMA interface with no DSP intervention. After all relevant data have been read, the acquisition system drives the DSP IRQ1 interrupt signal (one of the local bus signals on the mother-board) thus instructing the DSP to rearm the channel for a new trigger, as shown on the left side of Fig. 4.

Hardware settings and algorithm parameters can be accessed using a dedicated “slow control” interrupt routine associated to the IRQE interrupt signal (see Fig. 4).

6. Semi-Gaussian shaping: a study case

A few analysis routines have been written for the DSP, in ADSP21xx assembler language. At first, work has been done to implement on DSP the calculations previously performed off-line including constant fraction timing (either using linear or cubic interpolation), gated integration, amplitude estimation [1–4].

One peculiar task is to reproduce the behaviour of the standard analog semi-Gaussian shaper employed since a few years at the GARFIELD apparatus for CsI(Tl) signals. The DSP algorithm had to closely reproduce the analog shaper set to the shaping constant and pole zero values employed during measurements. This requirement was called for in order to simplify and speed up the calibration of the data collected with digitizing electronics, expected to substitute the analog shapers.

An Infinite Impulse Response (IIR) filter algorithm [17] has thus been written and tested. A custom fit procedure for signal analysis would have been more appropriate, but was not deemed necessary for a study of this kind.

---

**Fig. 4. Flow chart of a DSP algorithm.**

Please cite this article as: G. Pasquali, et al., A DSP equipped digitizer for online analysis of nuclear detector signals, Nuclear Instruments and Methods in Physics Research A (2006), doi:10.1016/j.nima.2006.10.008
based on DE (“Differential Evolution”: a population-based, stochastic function minimizer [18]) has been used to model filter response on that of GARFIELD analog shapers while keeping the calculation time as small as possible by reducing the number of poles and zeros in filter’s system function. The filter is implemented as a constant–coefficients difference equation [17], whose coefficients are determined by the fit. The fit also takes into account the finite (16-bit) precision of filter coefficient representation in DSP memory. The calculation is carried out using 32 bits words (the DSP ALU works on 16-bit operands) in order to get the desired filter stability and precision. A satisfactory filter calculation time of about 50 μs was obtained by performing a moving average on the signal followed by a decimation by 16 before filtering. Averaging and decimation do not sensibly worsen the final resolution. The \( \mathcal{Z} \)-transform of the adopted filter has the form

\[
\mathcal{Z}(z) = \frac{b_0 + b_1 z^{-1}}{1 - a_1 z^{-1} - a_2 z^{-2} - a_3 z^{-3}}.
\]

To take decimation into account, coefficients had to be calculated for a 128 ns sampling period. Their values are shown in Table 1.

In order to compare the two filters (analog and digital IIR), the same “detector-like” pulser signal (a step with variable rise-time followed by an exponential decay, as those produced by typical charge sensitive preamplifiers) was fed to both the analog shaper and the digitizer. The output of the analog shaper was also sampled and stored. In Fig. 5 we show the output of the analog shaper (sampled at 8 ns period and appearing as a continuous line in the figure) and the output of the IIR filter (appearing as a stepped line, due to the decimation operated by the DSP, effectively increasing the sampling period to 128 ns) for a few values of the input signal’s rise time (ranging from 50 ns to 5 μs). The IIR filter closely follows the analog one, also for different rise times of the input signal.

### 7. Pulse shape discrimination in CsI(Tl)

The pulse shape discrimination algorithm mimics a well-known analog method, sketched in the upper half of Fig. 6.

The detector signal is fed in parallel to two filters of different time constants, a “fast” shaper and a “slow” shaper. The analog chain at the top of Fig. 6 is replaced in our case by the much simpler chain sketched in the bottom half of the figure and the two filters are calculated by the DSP. The calculated “fast” shaper is a semi-Gaussian filter with \( \tau = 700 \) ns, the calculated “slow” shaper is the filter described in Section 6, having a peaking time of about 6 μs.

The amplitudes of the filtered signals \( A_f \) and \( A_s \) are stored for the off-line analysis.

A “fast-slow” correlation—actually \( A_f \) vs. \( (A_s - f \cdot A_f) \) where \( f \approx 4 \) is shown in Fig. 7. Hydrogen and helium isotopes are clearly resolved. The data were obtained from one of GARFIELD’s CsI(Tl) detectors in a physics run recently performed at LNL, exploiting the reaction \( ^{32}\text{S} + ^{56}\text{Fe} \) at 16.5 MeV (ALPI accelerator). About 200 digitizing channels have been used in the experiment and a PSA quality similar to that of Fig. 5 is obtained for all the CsI(Tl) scintillators of GARFIELD. In Fig. 7, the curves associated with different light particle isotopes can be followed down to the point where they merge (corresponding, e.g. to \( A_f \approx 200 \) for hydrogen isotopes). The trigger threshold of the digitizer (see Section 3.3) sets a lower limit on \( A_f \) values at \( A_f \approx 80 \), as evidenced in the inset. Therefore, for GARFIELD’s CsI(Tl) detectors, the region where light particle isotopes can be identified is not limited by the digitizer threshold.

### 8. Conclusions and future developments

A VME system aimed at digitizing and processing detector signals has been designed and implemented. The

---

**Table 1**

Coefficients of the IIR filter (see Eq. (1))

<table>
<thead>
<tr>
<th>( b_0 )</th>
<th>( b_1 )</th>
<th>( a_1 )</th>
<th>( a_2 )</th>
<th>( a_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.86560 \times 10^{-3}</td>
<td>-7.86920 \times 10^{-3}</td>
<td>2.88372</td>
<td>-2.77450</td>
<td>0.890655</td>
</tr>
</tbody>
</table>
design is modular, consisting in a multi-channel mother-board on which up to eight digitizing daughter-boards can be plugged. Data readout can be performed either via VME bus or via the faster FAIR bus. Each daughter-board is equipped with a 12-bit, 125 MSamples/s ADC and a DSP for on-line processing of detector signals. About 200 channels and 30 mother-boards have already been built and installed and they are presently in use at the GARFIELD apparatus in LNL-Legnaro.

Work is currently under way to implement a new type of daughter-board where a FPGA will be used to implement the on-board trigger, instead of the two comparators presently used. The FPGA will continuously receive the samples produced by the ADC, performing filtering and trigger logic on the digitized signal.

A prototype digitizing channel compatible with our mother-boards and including a much faster digitizer based on an analog pipeline [19] is also being developed in collaboration with IN2P3 in the framework of FAZIA [20], a project for R&D of a next generation apparatus for nuclear physics experiments.

References


Fig. 7. Pulse shape discrimination of light charged particles in CsI(Tl) performed by the on-board DSP; the reaction was $^{32}$S+$^{56}$Fe at 16.5 AMeV.