The CMS Silicon Tracker is going to be the largest silicon detector made so far, with about 210 square meters of sensitive area. The CMS Tracker collaboration, after the completion of the R&D phase, has put a lot of effort in finalizing the design of the silicon sensors, electronics hybrid, APV chip and many other crucial components in order to make such a detector possible. Many laboratory tests and test beam studies have been done. The project is now moving toward mass production. In this paper an overview of the CMS Silicon Tracker is made describing many of the progresses made on basics components of the Silicon Tracker.

1. Introduction

The CMS Tracker is the main tracking detector of the CMS experiment. It has to guarantee a transverse momentum ($p_t$) relative resolution of 15% for a particle of 1 TeV/c momentum, a high track reconstruction efficiency of about 95% for isolated tracks in a large rapidity range and to provide a good two track separation in order to cope, at small distance w.r.t. beam intersections, with the high track density determined by the energy and luminosity of the LHC collider. All these requirements are necessary to guarantee the discovery of a high mass higgs and the search for new particles.

Moreover the tracker has to cope with the high radiation fluences cumulated during the many years of running at LHC. The CMS collaboration has adopted a full silicon tracker[1] made by a vertex realized in pixel technology (Pixel Detector) and a main tracking detector composed of silicon strip modules (Silicon Strip Tracker, SST).

The silicon detectors technology is well established and has been successfully used in several past and present experiments. On the other hand, the SST is more than one order of magnitude bigger than ever made silicon trackers, with about 210 meter square of sensitive area and 9.6 million channels, therefore is a very challenging project.

Here it will be presented the general structure of the detector and the status of few crucial components of the SST: sensors and front end hybrids. It will follow the present understanding of the module performances.

2. SST structure

A full description of SST can be found in [1]. Here only the main ideas that make the project to look as it is will be explained. A sketch of a quarter of the detector is visible in figure 1. There are four main structures: Inner Barrel (TIB) and Outer Barrel (TOB) are organized in cylinders and use rectangular silicons; Inner Disks (TID) and Endcaps (TEC) are organized in disks and use wedge shaped silicons. All modules use single sided silicon sensors but about half of the layers use back to back modules with both $R\phi$ and stereo measurement in order to provide a three dimensional measurement of the track hit element, limiting the number of ghosts. Different silicon (and therefore module) microstrip geometries have been adopted, with increasing strip pitch (80 to 200 $\mu$m) and length (9 to 20 cm) moving from the lower to the higher radius in order to optimize the number of readout channels: the increase of noise determined by the higher capacitance load of outer silicon sensors has been compensated with a larger signal collected in a thicker substrate: 300 $\mu$m for $R < 50$ cm and 500 $\mu$m for $R > 50$ cm. Silicon resistivity has been chosen according to expected fluences, therefore
lower (1.5-3 kΩ cm) for thin and higher (3.5-7 kΩ cm) for thick silicons. There are in total 14 different sensors designs.

Results of simulation studies[2] on SST performance are shown in figure 2. The efficiency for isolated is very high for the full angular coverage of the tracker; the lower efficiency for isolated hadrons is due instead to interaction with the tracker material. Momentum measurement precision is of 10% for a 1 Tev/c particle.

2.1. Sensors

All silicon sensors are single sided p+ on n microstrip detectors, AC coupled with polysilicon bias resistors of 1.5 MΩ, the width/pitch ratio of the p+ strip has been taken equal 0.25 and left constant along the strip length also for wedge geometries. The metal strip is larger than the p+ implant by 4-8 µm since it has been shown to enhance the stability at high biases[3].

The two manufactures considered for the silicon sensors production are Hamamatsu Photonics (thin sensors) and STMicroelectronics (thick sensors). They have provided the first preseries of sensors and are now under evaluation by the SST collaboration. Full testing is done on all sensors received to determine their quality and also the processing quality is checked using test structures, before and after irradiation. The full testing procedure is described in [4].

Measurements are made, for each sensor, of total leakage current and depletion voltage and, for each strip, of single current, coupling capacitance and polisilicon resistance.

Hamamatsu sensors accepted by these tests are more than 99% of a total of about 280 pieces and therefore are qualified for production.

STMicroelectronics sensors have been more problematic since they have shown an average accepted fraction of about 50-60%. Recently (autumn 2002) STMicroelectronics has improved the quality control procedure and this, together with a better tuning of the processing, has determined a 90% acceptance in batches. If this results will be confirmed in next batches also STMicroelectronics will be fully qualified for production.

Proton irradiation tests have been attempted on test structures. Results on the dependence of depletion voltage on the fluence are shown on figure 3 both for thin and thick silicon baby sensors, together with the Hamburg model predictions: for both thickness sensors reach a depletion
Figure 2. SST performances from full simulation studies: single particle track reconstruction efficiency (muons and pions at top left and right respectively); $p_t$ resolution (bottom left) and reconstructed higgs signal for $m_H = 130 \text{ GeV/c}^2$, $H \rightarrow Z^* Z^*$ ; $Z \rightarrow \mu^+ \mu^-$.

Voltage of about 300 V after 10 years of LHC at full luminosity, taking already into account a 50% safety factor. Moreover results are in agreement with the model and this proves that fabrication processing is well understood and under control by manufacturers. The leakage current dependency on fluence is shown on figure 3 and is found to be as expected: this proves that the dose given to silicon sensors during the irradiation test was well estimated. A choice made by the SST collaboration was to use a silicon substrate with $\langle 100 \rangle$ crystal lattice orientation, since it has shown to guarantee that interstrip capacitance does not increase with fluence[3]. This is important to maintain good signal over noise performances of silicon modules during the several years of LHC running. Hamamatsu detectors have confirmed to have no dependence of interstrip capacitance w.r.t to the irradiation fluence. STMicroelectronics sensors have not all shown such a property. This has been understood to be correlated with the quality of the SiO2 growing process, quantified as number of fixed charge trapped at the interface and therefore it can be checked by the measurement of flat band voltage, $V_{fb}$ on MOS structures. In fact if SiO2 quality is not good enough, even with $\langle 100 \rangle$ orientation there is an increasing $C_{int}$ with fluence. This correlation is clearly visible in figure 3 where $C_{int}$ is shown before and after irradiation for different values of $V_{fb}$: clearly for $V_{fb} \leq 7V$ there is no effect after irradiation. In the qualification of silicon batches a maximum value of $V_{fb} = 10V$ has been introduced and STMicroelectronics will deliver to SST only sensors satisfying this selection.
2.2. Hybrid

The front end hybrid is a crucial component of the SST, it has to: house the front end chips (APV25[6], APVMUX, PLL and DCU); provide a good thermal dissipation to allow the heat transfer (3 Watts maximum) from the chips to the module carbon fiber frame; operate down to -20 C degrees; be rigid and flat within 100 µm to allow automated assembly; be radiation-hard. Four metal layers separated by maximum 180 µm are implemented and no bias HV is going through the hybrid.

The hybrid realization was firstly made using a ceramic substrate with copper lines. It began on early 2001 and the first working release was ready for summer/autumn 2001 in a number of about 180 pieces. The design principle showed to work correctly for what concern noise performances, irradiation tests and thermal cycles. The production yield was about 80% but was not optimal for mass production, mainly because the soldering of the kapton cable to the ceramics has shown to be problematic and not very reliable.

Secondly, it was attempted an advanced FR4 printed circuit board technology. This solution is very cheap and was made possible by solving two important problems: the difference of CTE with the carbon fiber frame, by using a soft glue.
Figure 4. The main hybrid technologies attempted for SST front end electronics: (left) on ceramic, (centre) on FR4/kapton; (right) scheme of the finally accepted solution consisting of full flex kapton on ceramic or carbon fiber support.

like silicon one; the low thermal conductivity by inserting in FR4 substantial number of copper joints from the top to the bottom layers. Unfortunately, the yield of production showed to be quite low and still remained the problem of soldering the kapton cable, therefore this solution was abandoned quite quickly.

Thirdly, much better performances were obtained substituting the two top layers of the hybrid with polyimide, laminated on the FR4, and therefore getting a full integration of the cable on the hybrid. This solution (called flex/rigid) has shown to be reliable and robust and several tens of hybrids were made. The process of lamination, being made at high temperature, determined in many hybrids non-planarity of up to 200 microns. This made the automatic assembly of the module quite problematic and therefore a better solution was searched.

Finally, a full kapton solution was attempted, with two layers of polyimide, adopting a ceramic or a carbon fiber substrate only as mechanical support and heat transfer. The kapton is glued to the support at nearly room temperature, using epoxicid glue, while the connection to carbon fiber frame is done using a soft glue. This final solution has been used to produce few tens of hybrids giving very satisfactory results. It is the solution adopted for the production of SST hybrid.

Three out of the four different technologies are shown in figure 4.

At the same time also the ASICS chip mounted on the hybrid other than the APV25, have been also improved.

3. Module performances

The modules produced have been so far realized in only three geometries, one per SST sub-detector: first TOB layer, sixth TEC ring and third TIB layer (figure 5). On these three module types many studies on performances have been made using test beam.

An interesting test was done on October 2001 using CERN X5 beam with 25 ns bunch structure, similar to LHC conditions, and 120 GeV pions. Six TOB modules where exposed: signal to noise ratios of about 30 and 20 were measured with APV25 chip running in peak and deconvolution mode respectively, in agreement with expectations. The noise distribution of all modules was checked to be of gaussian type up to four sigmas and cluster reconstruction efficiency was measured to be very high, about 99%.

3.1. Module response to HIPs.

During this test beam it was discovered the saturation of a full APV25 chip[6] when a very high signals generated by a highly ionizing particle (HIP) was delivered to the silicon. HIPs are particles interacting with the material and generating a small shower[7]. An event of these kind is
Figure 5. TK modules produced so far (shown at 1:3 scale): 25 units of 1-st layer TOB type (left); 13 units of 6-th ring TEC type (center) and 11 units of 3-rd layer TIB type (right).

shown in figure 6 where it is visible the response of all silicon modules: a single particle go through the first six modules (starting from bottom) then a shower is formed causing the saturation of the corresponding APV25 chip on the seventh module and still many tracks are visible in the following detectors. Chips detecting the signal of a HIP stay in saturation for few hundred ns. For this test beam HIPs were found to be at $4 \times 10^{-4}$ level.

The magnitude of a HIP signal is sufficient to saturate channels hit and due to a crosstalk with all other channels, caused by the biasing scheme of the APV25 chips in the hybrid, the entire chip goes to saturation for some time. In the hybrid all preamplifier inverter stages of one chip are derived from the 2.5 V bias line via a common 100 $\Omega$ external resistor ($R_{int}$), and this cause the crosstalk. This feature of the hybrid was introduced to avoid chip oscillations and kills common mode noise, but in case of a HIP it causes a dead time during which the chip stays blind.

The lost of hit reconstruction efficiency due to HIP events rate, extrapolating the CERN X5 results to CMS conditions and running APV25 in peak mode, is estimated to be below the 0.2 %[8].

Another test with a high intensity beam of 300 MeV pions was done more recently at PSI to better study the effect of HIPs in conditions closer to CMS at LHC: better determine the rate and measure the dead time for different modules geometries (TOB, TEC, TIB) and different values of $R_{int}$ and study the behaviour in deconvolution mode.

Data analysis is still going on, therefore only preliminary results are available. On figure 5 the time evolution of the baseline shift due to a HIP is shown for the different configurations and APV25 running in peak mode: the dead time is about 100 ns, followed by a recovery time of nearly 250 ns and an overshoot greater than 400 ns. In the same figure it can be noticed that if $R_{int}$ is reduced to 50 $\Omega$ dead time, recovery and overshoot time are
reduced for a total gain of about 150 ns.

3.2. Pinholes effect.
A similar effect to that caused by HIPs on the APV25 electronics can be determined by pinholes, i.e. silicon strips that are coupled in DC to the electronics because the SiO$_2$ layer on top of the p' diode is broken.

This effect has been studied in laboratory and results show that a sensible deterioration of signal is visible when at least two pinholes are present on the same APV25 chip, considering a leakage current of µA per strip, as in the last year of LHC. If $R_{int} = 50$ Ω is adopted, the number of pinholes tolerated by an APV25 chip becomes seven. The CMS Tracker community is considering to lower to this value $R_{int}$, the only drawback being an increase of low voltage current of about 5-10 %.

4. Test of equipped substructures
From the last quarter of year 2001 to the end of 2002, several progresses were made on the understanding of SST substructures, beginning to perform test of sub-systems partially equipped with modules.

The first TOB rod was equipped with six modules and studies on grounding scheme and cooling were done. Tests made with radiation sources and noise measurements show a signal to noise ratio very close to that obtained in single module tests, reading out the signal with the optohybrid. Similarly a partial equipment of a TEC petal was done using four modules and no degradation of results was found with respect to single module tests.

For TIB, first tests were done using prototypes of final power supply and the full length of 150 meter cable to supply power to three TIB modules mounted on a prototype mechanical structure, as in CMS: no signal nor noise degradation was found. Moreover tests were done on over-voltage behavior on the 2.5 V line, due to switching off of preamplifier bias of APV25 chips of modules when sending a system reset signal. A tolerable over-voltage of less than 0.1 V was found, with no arm to the APV25 chips.
5. Conclusions

The CMS Tracker is a fundamental part of the CMS experiment. During 2002 the Silicon Strip Tracker has entered into production of a few components. Sensors preseries were tested and gave good results in the many silicon geometries of SST; a final technology for the front end electronics was found and system tests have given the first good results showing that the full front end electronics chain works correctly with a remote power supply as in the present CMS Tracker scheme. Mechanical structures are also entering into production.

So far, about 50 modules subdivided into three different geometries (TOB, TEC and TIB) have been built following an almost completely final production scheme. Several tests on those modules were done: in particular test beam data have given many useful informations on their performances under an LHC like beam. HIP events have been found to cause a dead time in APV25 chip of a few 100 ns, but their rate in CMS will determine a negligible decrease of efficiency.

All this allows the SST detector to enter during 2003 firstly into full module production and secondly into the beginning of the assembly of full mechanical structures.

REFERENCES