Recent results with CCDs for the Linear Collider

Steve Worm
Rutherford Appleton Laboratory

for the Linear Collider Flavour Identification (LCFI) Collaboration
Outline

- The International Linear Collider
- LCFI activities
  - Column-parallel CCDs
  - CPC2 results
  - Readout chip development
  - ISIS developments and results
- Future prospects
The International Linear Collider

- Detector parameters driven by the physics needs
  - ILC is built for *precision* physics; reflected in detector
  - Vertex detector must identify b, c, tau decays, also charge
  - Coverage to far forward, ultra-low mass

- Detector must fit the environment and construction constraints
  - How to get services in, cables and heat out
  - Operational environment must be understood
  - Can the beam structure be exploited?

- The construction timescales
  - Detector TDR by 2008-2009?
  - Detailed vertex design can come later
  - Aim for vertex detector technology choice by ~2010
Tracking and Timing Features at the Linear Collider

What sort of tracking and vertexing is needed for the Linear Collider?

- Vertex detectors for the Linear Collider will be *precision* devices
  - Need very thin, low mass detectors
  - No need for extreme radiation tolerance
  - Need high precision vertexing \( \rightarrow \) eg \( \sim 20 \) μm pixels
  - Can not simply recycle technologies used in LHC or elsewhere

- High pixelization and readout implications
  - \( 10^9 \) pixels: must break long bunch trains into small bites (2820/20 = 141)
  - Read out detector many (ie 20) times during a train
  - ...or store info for each bite and read out during long inter-train spaces

---

**Bunch Train**

**Bunch Spacing**

\[ \text{Bunch Train: } 0.2 \text{ s} \]

\[ \text{Bunch Spacing: } 0.95 \text{ ms} \]

\[ 337 \text{ ns} \]

\[ x2820 \]
ILC Vertex Detector

- Detector not yet determined; sensor technology not chosen yet
  - Many sensor options: CCDs, DEPFET, CMOS pixels, FP-CCD, etc...
  - Many new ideas being developed (see Ringberg Workshop)
  - It is too early to choose; no need to yet!

- Fast (column-parallel readout) CCDs
  - Sensor+layout concept actively being developed
  - 20 μm x 20 μm pixels in 5 layers
  - ~10⁹ channels
  - Inner radius 1.5 cm
  - Readout time 50 μs
  - Ladder thickness 0.1% \( X_0 \)
Column-Parallel CCDs

- **Fast Column-parallel CCDs (CPCCD)**
  - CCD technology proven at SLD, but ILC sensors must be faster, more rad-hard
  - Readout in parallel addresses speed concerns
  - CPCCD's feature small pixels, can be thinned, large area, and are fast
  - CPC1: two-phase, 400 (V) x 750 (H) pixels, each $20 \times 20 \mu m^2$

Column Parallel CCD
Readout time = $\frac{N}{F_{out}}$

"Classic CCD"
Readout time = $N \times M/F_{out}$

Bump-Bonded CPCCD + Readout

CPCCD1 (e2v)
Column-Parallel CCDs: CPC1 results and CPC2 design

- First-generation tests (CPC1):
  - Noise ~100 e⁻ (60 e⁻ after filter).
  - Minimum clock potential ~1.9 V.
  - Max clock frequency above 25 MHz (design 1 MHz).
  - Limitation caused by clock skew

- Next generation in production (CPC2):
  - Busline free design (two-level metal)
  - Large area 'stitched' sensor, choice of epi layers for varying depletion depth
  - Range of device sizes for test of clock propagation (up to 50 MHz)
  - Large chips are nearly the right size

Steve Worm - LCFI
October 1, 2006
CPC2: Next generation CCD

- CPC2: second generation Column-parallel CCD
  - 6 wafers: single-metal (100 Ω cm @ 25 µm and 1.5 kΩ cm @ 50 µm)
  - Yield: 71% for CPC2-10, 63% CPC2-40, 25% CPC2-70
  - 4 more wafers with 2-level metal (busline-free) in post-production
  - Busline-free variant designed for 50 MHz operation
  - Another 10 wafers in pipeline

→ Busline-free design a big step!
First Data from CPC2

- **CPC2-10** (low-speed version)
  - $^{55}$Fe spectrum below at -40C, 500ms integration time, 1MHz clock
  - Noise too high-- external electronics suspected
  - Double-metal busline-free CPC2 (high speed version) expected soon

→ Testing complete for CPC2 single-metal; works well
Capacitance Reduction Ideas for CCDs

- **High capacitance CCD is challenging to drive**
  - 40 nF and ~2V clocks @ 50 MHz... ≥20 amps!

- **Working to reduce capacitance (and drive voltage)**
  - Inter-gate capacitance ($C_{ig}$) is dominant; depends on gate and overlap sizes
  - New sensor designs (open phase, pedestal gate, and “Christmas tree”) can reduce $C_{ig}$ by factor of ~4?

→New test structure to test these ideas (early 2007)
Readout Electronics: CPR2 Readout Chip

- Designed to match the Column Parallel CCD (CPC2)
  - 20µm pitch, maximum rate of 50MHz
  - 5-bit flash ADC, on-chip cluster finding
  - Charge and voltage inputs

- Features for the CPR2 include
  - Cluster Finding logic, Sparse read-out
  - Better uniformity and linearity
  - Reduced sensitivity to clock timing
  - Digital and analogue test I/O
  - Variety of test modes possible
  - 9.5 mm x 6 mm die size, IBM 0.25µm

→ Major piece needed for a full module
CPR2 Readout

- **CPR2 sparsification**
  - Cluster finding with 2x2 kernel
  - Global threshold
  - 4x9 pixels flagged for readout
  - Several minor problems

→ Chip works!

- **CPR2 Dead Time and Cluster Separation**
  - Design occupancy ≤1%
  - Errors as distance between clusters decreases → deadtime
  - Extensive range of improvements for next version (CPR2A)

→ Design of CPR2A has started
**In-Situ Storage Image Sensor**

- **ISIS Sensor details:**
  - CCD-like charge storage cells in each pixel, CMOS or CCD technology
  - p+ shielding implant (or epi) forms reflective barrier

- **Operational Principles:**
  - Charge collected at photogate, transferred to storage pixel during bunch train
  - 20 transfers per 1ms bunch train
  - Readout during 200 ms quiet period after bunch train
ISIS Properties and Status

**ISIS advantages:**
- Low frequency clock -> easy to drive
- 20 kHz during capture, 1MHz readout
- \( \approx 100 \) times more radiation hard (fewer charge transfers)
- More robust to beam-induced RF pickup

**Process and Status:**
- Combines CCD and active pixel technologies
- Deep implant or custom epi needed
- Overlapping poly?
- Investigating CMOS and CCD vendors

\( \rightarrow \) Proof of principle device (ISIS1) manufactured
The ISIS1 Cell

Array and Cell details
- 16x16 array of ISIS cells with 5-pixel buried channel CCD storage register
- Cell pitch 40 $\mu$m x 160 $\mu$m
- No edge logic (pure CCD)
- Chip size 6.5 mm x 6.5 mm

Output and reset transistors

Photogate aperture (8 $\mu$m square)

CCD (5x6.75 $\mu$m pixels)
**ISIS1: Test Results**

- $^{55}\text{Fe}$ test results
  - ISIS1 without p-well works fine
  - Top row and 2 side columns not protected and collect diffusing charge
  - Bottom row is protected by output circuitry
  - ISIS1 with p-well has large transistor thresholds, permanently off

→ Will re-manufacture p-well structure (e2v)
Radiation Damage effects in CCDs

Simulation of Charge Transfer
- Full 2D simulation in ISE-TCAD
- Count signal e⁻ trapped in pixel
- CPU-intensive and time consuming
- Simple analytical model gives similar results
- Window of low charge transfer inefficiency (CTI) between -40 °C and 0 °C
- Needs experimental verification

→ Very important for operation
Conclusions

- Column-parallel CCD
  - Second generation high speed CCD: CPC2
  - Expecting bump-bonded CPC2+CPR1+CPR2 assemblies soon
  - Active program for capacitance and clock amplitude reduction
  - Third-generation readout ASIC available, new one under design

- In-situ Storage Image Sensor
  - Proof of principle device works
  - New structures being produced (p-well)
  - Design of small-pixel ISIS2 will begin next year

CCD development for the ILC progressing well!
Clock drive for CPC2

- Transformer-based driver
  - Designed for 2 Vpeak-to-peak at 50 MHz and 40 nF (i.e. for CPC2-40)
  - Planar air-core transformers on 10 layer PCB, 1 cm²
  - Parasitic inductance of bond wires a major effect
  - Should work with “busline-free” CPC2

- CPD1 driver ASIC
  - Designed for either large or small sensors: 40 nF/phase at 50 MHz or 127 nF/phase at 25 MHz
  - One chip drives both phases with 3.3V clock swing, 21 amps/phase
  - 0.35 m CMOS process
  - 3 mm x 8 mm size