Serial Powering of Silicon Strip Modules for the ATLAS Tracker Upgrade

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Outline

• Serial Powering scheme
• Stave results
• Serial powering developments
• Conclusions
Powering schemes issues

In SCT there are 4088 Detector modules

Independent powering:

4088 cable chains
22 PS racks
4 crates / rack
48 LV and 48 HV channels/crate
Installation is a major logistical challenge

Power dissipated in cables:
Overall efficiency 40%
Powering schemes comparison

Efficiency ratio: serial over independent powering

Example of SP efficiency plot
vs. number of modules (N)
and supply voltage (V) for \( I_m = 2 \text{ A} \) \( R_c = 3 \Omega \)

SP Efficiency:

\[
\eta_{SP} \approx \frac{P_M}{P_M + P_C} = \frac{1}{1 + \frac{I_m R_c}{N V_m}} = \frac{1}{1 + \frac{x}{N}}
\]

IP Efficiency:

\[
\eta_{IP} \approx \frac{P_M}{P_M + P_C} = \frac{1}{1 + \frac{N I_m R_c}{N V_m}} = \frac{1}{1 + x}
\]

\[ P_c = I_m^2 R_c \quad P_M = N I_m V_m \quad P_c = N I_m^2 R_c \quad P_M = N I_m V_m \]
In a Serial powering scheme the power source (Current source) provides power to the chain of shunt regulators, which provide power to the local modules. DAQ communication is achieved through AC coupled LVDS.

Parallel topology transforms into Serial topology through Norton transformation.

**Topological issues have their counterpart in the complementary topology (i.e. short in PP equivalent to break in SP)**
Powering diagram - efficiency -

<table>
<thead>
<tr>
<th></th>
<th>$I_{sm}$</th>
<th>$V_{drop}$</th>
<th>$V_s$</th>
<th>$P_{cab}$</th>
<th>Efficiency: $P_{sm}/P_{total}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP</td>
<td>NI</td>
<td>IR</td>
<td>V</td>
<td>NI$^2$R</td>
<td>$1/[1 + x]$</td>
</tr>
<tr>
<td>PP</td>
<td>NI</td>
<td>NIR</td>
<td>V</td>
<td>N$^2$I$^2$R</td>
<td>$1/[1 + Nx]$</td>
</tr>
<tr>
<td>SP</td>
<td>I</td>
<td>IR</td>
<td>NV</td>
<td>I$^2$R</td>
<td>$1/[1 + x/N]$</td>
</tr>
<tr>
<td>DC</td>
<td>NI$^2/G$</td>
<td>NIR$^2/G$</td>
<td>GV</td>
<td>N$^2/I^2R$</td>
<td>$1/[1 + xN/G^2]$</td>
</tr>
</tbody>
</table>

- in SP efficiency increases with N
- in /SP efficiency decreases with N (high G is needed in DC$^2$)
Serial powering - floating ground and HV -

Alternative HV powering: one HV supply per M modules

Standard HV powering: one HV per module

• In SP it is possible to use **single HV supply for several sensors**

• Dynamically each sensor is grounded to current source ground through output impedances of shunt regulator ‘below’

• Low shunt output impedance crucial to achieve good ‘grounding’ and reduce noise
• **Parallel scheme**
  - Use each ABCN’s integrated shunt regulator
  - Use each ABCN’s integrated power transistor(s)

• **Multi drivers scheme**
  - Use one external shunt regulator
  - Use each ABCN’s integrated power transistor(s)

• **SPI - like scheme**
  - Use one external shunt regulator
  - Use one external power transistor
  - *Most similar to what has been used with ABCD…*
Serial powering circuitry evolution

SSPPCB - 2006/7 -
38 mm x 9 mm

SPPCB - 2006 -
111 mm x 83 mm

SPSCT - 2005 -
150 mm x 150 mm
Serial powering stave implementation

- Based on CDF stave design
- Uses several CDF “spare parts”
- New bus cable (LBNL)
- New thick film hybrid (LBNL)
  - With 4 ABCD chips
- New serial powering PCB (RAL)
- Two staves have been built
- One at LBNL (C.Haber)
- One at RAL
- The interface PCB carries a connector
- All other connections are wire bonds
- Picture shows stave assembled at RAL
- “Module 2” left as hybrid for better comparison with single hybrid data
Results agree with expected ABCD performance
Thirty modules Stave

A chain of 30 hybrids: Power input 123V, 0.8A

Thick Film Hybrid for 6 ABCD chips with integrated Serial Powering circuitry: requires ~0.75A at 4V

Carl Haber, LBNL
Thirty modules stave

- 7 modules and 2 hybrids mounted and tested on the stave
- Leakage current is stable
- Noise performance improves on stave, all are 900 electrons
- Group of 5 modules share a common command line all read out together
Thirty modules stave: preliminary results

- Threshold vs. Channel number
- VT50 (mV)
- Gain (mV/fC)
- Output Noise (mV)
- Input Noise (ENC)
- Scan point vs. Occupancy
- S-curve
ABC-Next

- New front end chip for ATLAS upgrade Silicon Strip module
- 250nm CMOS IBM
- 2.5V digital / 2.2V analogue
- binary architecture
  - 128 channels of preamplifier/shaper/comparator
  - 25nS peaking time
- Novel powering schemes
  - On chip shunt regulators
  - On chip linear regulator for analogue supply
  - Due back in October 08

Jan Kaplon ABCN FE Chip for ATLAS Inner Detector Upgrade, TWEPP 2008
Generic Rad-hard Serial powering ASIC – SPI -

- Multi-purposes Serial Powering Interface for scheme 2 and 3
- Designed for generic SP use, but of great interest to ATLAS strip community
- Programmable shunt regulator (1.5…2.5V, >1A)
- Two linear regulators (1.2…2.5V 500mA)
- Power on Reset
- Integrated Monitoring of current
- 7 AC-coupled LVDS comports
- Rad tolerant design TSMC 0.25um

Specifications provided by RAL – M.Trimpl The SPI (Serial Powering Interface) chip TWEPP 2008
Further Serial Powering Activities

• Continued integration on supermodules

• SP features in Pixel FE chip
  – Michael Karagounis Development of the FE-I4 pixel readout chip TWEPP 2008

• Development of SP protection schemes
  – D Lynn, J Kierstad, BNL
  – A. Eyring, Bonn
  – G. Villani, RAL

• Constant Current Source development
  – J. Stastny, Prague AS
Conclusions

• Serial Powering scheme has been shown to perform well
  – 6 and 30 module staves
  – 6 SCT modules
  – Excellent noise performances
• Next generation ASICs for ATLAS strip modules integrate SP features
• Dedicated ASIC for SP
• System issues currently being addressed
  – Custom current source
  – Protection schemes
• The shunt regulator output has to carry the all current in case of load disconnected, to guarantee functioning of the chained modules

• This condition implies a power dissipation by the shunt device directly proportional to its voltage output thus power wasted and risk of damage if not cooled or over dimensioned

• A method investigated relies on automatically reducing shunt output voltage in case of overcurrent condition

• This feature could also be digitally enabled to turn off a module
Backup slides: Over current condition - Thermal analysis

Thermal analysis of SSPCB01 using IR camera 8...13μm

- Simulated faulty condition:
- No clock present onboard
- No cooling
- Different biasing conditions (400, 500, 600)mA

* SSPPCB01 was left running at 700mA for 30mins. No change in performances or damaged observed afterwards.
• The regulator automatically lowers its output voltage (from 4V to 1V in the test circuit) if the current through the power PNP continuously exceeds a set threshold for a set amount of time

• The voltage output recovers with hysteresis (≈ 150mA in the test circuit)

• The power pulse following an over current is not long enough to damage the PNP transistor

• By proper design the power PNP is housed in SOT23 package, no heat sink needed
**Test results:**

- Voltage decreases from 4V to 1V within 3 ms following an over current (40mA to 1500mA).
- Voltage output recovers to 4V from 1V (slew rate limited) within 70 ms.
- With output voltage 1V the power dissipated by the PNP is \( \approx 0.32 \text{W} \). Noise \( \approx 2\text{mV} \).
- Circuitry left running for >1hr @ 1.5A. No damage or change in performances seen afterwards.
Backup slides: Power efficiency comparison

- in SP efficiency increases with N
- in DC² efficiency decreases with N: high G is needed

\[
\frac{\eta_{sp}}{\eta_{dc^2}} = \frac{1 + \frac{xN}{a \cdot N^2}}{1 + \frac{x}{N}} \geq \frac{\eta_{sp}}{\eta_{dc^2}} \geq 1 \Rightarrow N \geq a \cdot G
\]

If N = 6 G >= 6
If N = 30 G > 33…

High voltage and radiation hardness