Thin Pixel development for the SuperB Silicon Vertex Tracker

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the SuperB project

- the SuperB Silicon Vertex Tracker
- Layer0 options for the Technical Design Report
- CMOS Monolithic Active Pixel Sensor (MAPS)
- hybrid pixels
- exploiting vertical integration for Layer0
- conclusions
The SuperB Project

- The physics case for a high luminosity BFactory is clearly established:
  - Flavour physics is rich, SuperB promises sensitivity to New Physics but a large statistics is needed → 50-100 ab⁻¹.

- First generation of BFactories (PEP-II and KEKB) exceeded their design goals (L ~1.2-1.7 x10³⁴ cm⁻² s⁻¹, integrated 1.2 ab⁻¹) but an upgrade of 2 orders of magnitude in luminosity is needed to get 50 ab⁻¹.

- Increasing luminosity by brute-force (higher currents) not viable:
  - wall plug power and detector background explosion;
  - effective limitation around 5x10³⁵ cm⁻² s⁻¹.

- The SuperB Italian accelerator concept allows to reach and exceed the luminosity threshold L =10³⁶ cm⁻² s⁻¹ with:
  - design based on 4 and 7 GeV rings (similar to damping rings for ILC);
  - moderate beam currents (~2A);
  - final focus (ILC-like) + Crab Waist technique (verified with tests on Dafne).

- This approach allows to (re-) use parts of existing detectors and machine components.
The SuperB Process

- All scientific reviews are positive. Presented to CERN Council and approved for preparatory phase.
- Growing international interest and participation with formal international collaboration being formed. Project structure defined.
- R&D is proceeding on various items (eg. SVT Layer0)
- Technical Design Report phase approved by INFN.
- MOUs signed with France, Russia and SLAC and a letter of support from Canada.
- SuperB inserted as first project in National Research Plan by the Italian Research Ministry!

NEXT STEPS

- Intermediate Progress Report preparation (now in final editing);
- Government approval expected very soon;
- Technical Design Report: spring 2011;
- Operation by 2015.
The SuperB Silicon Vertex Tracker

SuperB SVT based on BaBar SVT design for R>3cm. BUT:

BaBar SVT
- 5 layers of double-sided Si strip sensor
- low-mass design. \((p_t < 2.7 \text{ GeV/c})\)
- stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- resolution \(\sim 15 \mu\text{m} \) at normal incidence

1) reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) requires an improved vertex resolution (\(\sim \text{factor 2}\))
   - Layer0 very close to IP (@1.5 cm) with low material budget (<1% \(X_0\)) and fine granularity (50 \(\mu\text{m} \) pitch)
   - Layer0 area 100 cm\(^2\)

2) bkg levels depend steeply on radius
   - Layer0 needs to have high radiation tolerance
   - Layer0 subject to large bkg (>20x5 MHz/cm\(^2\), >3x5 MRad/yr)
**SuperB SVT Layer technology options**

**striplets option:** mature technology, not so robust against background occupancy.
- marginal with background rate higher than \( \sim 5 \text{ MHz/cm}^2 \)
- moderate R&D needed on module interconnection/mechanics/FE chip

**hybrid pixel option:** viable, although marginal.
- reduction of total material needed!
- reduction in the front-end pitch to 50x50 \( \mu \text{m} \) with data push readout (developed for DNW MAPS)
- FE prototype chip (4k pixel, ST 130 nm) tested

**CMOS MAPS option:** new & challenging technology.
- Sensor & readout in 50 \( \mu \text{m} \) thick chip!
- Extensive R&D (SLIM5-Collaboration) on
  - Deep N-well devices 50x50\( \mu \text{m}^2 \) with in-pixel sparsification.
  - Fast readout architecture implemented
- CMOS MAPS (4k pixels) successfully tested with beams.

**Thin pixels with Vertical Integration:** reduction of material and improved performance.
- Two options are being pursued
  - DNW MAPS with 2 tiers
  - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor
CMOS MAPS
(Monolithic Active Pixel Sensors)

the concept:

→ MAPS integrate the sensor element and the readout electronics in the same substrate;
→ signal is collected by a diode (n-well/p-epitaxial layer);
→ charges move by thermal diffusion to the n-well;

the advantages:

→ same substrate for detector & readout;
→ MAPS sensitive volume only 10-15 μm thick → minimal amount of material in the detection region w.r.t. hybrid pixels;
→ CMOS commercial process → low fabrication costs.
Deep N-Well sensor concept

The deep n-well is used as the collecting electrode that can be extended to obtain higher single pixel collecting charge;

A classical optimum signal processing chain for capacitative detectors can be implemented at pixel level: charge to voltage conversion done by charge preamplifier (gain independent of capacitance).
Implemented in ST 130 nm process

Proof of principle (APSEL0-2)
- first prototypes realized in 130 nm triple-well ST-Micro CMOS process

APSEL3
- 32x8 matrix with sparsified readout
- Pixel cell optimization (50x50 \( \mu m^2 \))
  - increase S/N (15\( \rightarrow \)30)
  - reduce power dissipation x2

APSEL4D: 4k (32x128) 50x50 \( \mu m^2 \) matrix
- first matrix with an in-pixel sparsification and timestamping + data driven readout
- pixel cell & matrix implemented with full custom design and layout
- sparsifying logic synthetized in std-cell from VHDL model
- periphery incluses a “dummy matrix” used as digital matrix emulator

beam test in Sep 2008
- prototype MAPS module + striplets

radiation tests up to 10 MRad
### APSEL4D

- In the active sensor area we minimized:
  - logical blocks with PMOS to reduce the area of competitive n-wells
  - digital lines for point to point connections to allow scalability of the architecture with matrix dimensions

- 4K(32x128) 50x50 µm² matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:
  - register hit MP & store timestamp
  - enable MP readout
  - receive, sparsify, format data to output bus

**S/N up to 25 with power consumption ~ 30 µW/ch**

- **Signal for MIP** (MPV) = 980e-
- **S/N=23**
- **Threshold dispersion** 60e-
- **Average gain** 860 mV/fC
CERN beam test results on APSEL4D

HIT EFFICIENCY

- Hit efficiency up to 92% with a threshold @ 400 e-
- Uniform efficiency across the matrix
- 300 μm and 100 μm thick chips give similar results
  - Difference @ 400e- among chip22 and chip23 due to a readout malfunction

The competitive n-wells in pixel cell steal charge reducing the hit efficiency → fill factor ~ 90%

- 2D MAPS: Efficiency improves adding multiple collecting electrodes around competitive nwells.
- 3D MAPS: (2 tiers for sensor&analog + digital) fill factor and efficiency can improve significantly.
hit intrinsic resolution has been measured from the residual distribution after subtracting the contribution of multiple scattering ($\sigma_{MS} = 5 \mu m$) and the track extrapolation uncertainty ($\sigma_{track} = 6 \mu m$)

hit intrinsic resolution independent of threshold

hit intrinsic resolution fairly agrees with expectation = $50/\sqrt{12} = 14.4 \mu m$

better resolution on y is an artifact of a poorly efficient pixel border
HYBRID PIXELS R&D

» prototype front end chip for hybrid pixel received in april and tested
  » ST 130 nm (single tier)
  » 32x128 pixels, 50x50 μm²

- use data push readout architecture developed for MAPS chip
  now optimized with target rate (100 MHz/cm²) for full chip size (~1.3 cm²)
- VHDL simulation: readout efficiency > 98% @ 60 MHz readout clock
- space time coordinates with time granularity 0.2-5.0 μs (BC clock)

» pixel sensor matrix ready and characterized (FBK-IRST)
  » N-on-N: P- spray isolation on n side and p implant on the back side
  » wafer thickness of 200 μm (FZ,HR Si)

» bump bonding with the FE chip with IZM Berlin and characterization with radioactive source in preparation for TDR.
A classical signal processing chain is implemented (no shaper)

→ comparator threshold common to all pixels
→ possibility to **inject** a charge up to 12fC in selected pixels
   ✔ MIP on 200 μm Si → 2.6fC

**post layout simulation:**

threshold dispersion: 350 e-, ENC: 120 e- (no sensor), gain: 45 mV/fC
(150 e- @ $C_D = 100fF$)
characterization of the FE chip

- threshold dispersion = 490 e-
- ENC = 70 e-
- gain = 42 mV/fC
  - gain dispersion ~ 5%

fairly good agreement with the post layout simulation

→ a threshold tuning is forseen for the next design of the analog cell
→ the noise is smaller than expected
3D technology options for the SuperB Layer0

from 2D to 3D MAPS

- less PMOS in the sensor layer ➔ improved collection efficiency
- more room for in-pixel logic ➔ improved readout architecture
- analog and digital blocks in 2 tiers ➔ minimize cross-talk
- more room for both analog and digital power and signal routing

3D Hybrid Pixel detector

- high resistivity sensor ➔ larger signal ➔ better trade off between S/N and dissipated power ➔ radiation hard

3D front end chip: (2 tiers) to be connected to high resistivity sensor through some more (bump bonding) or less (direct bonding) standard technique
The first 3D CMOS MAPS in the APSEL family

- first APSEL-like DNW MAPS (2 tiers) realized within the 3DIC Consortium to explore the 130 nm Chartered/Tezzaron process

- Test structures → 3x3 analog matrix
  - first optimization of analog cell and sensor layout for 3D version
- 8x32 MAPS matrix with APSEL4D readout architecture
  - data-driven sparsified readout + timestamp; MacroPixel based
  - in next version improved architecture exploiting 3D (i.e. remove MacroPixel)
The physics case for SuperB is clearly established, the project is good shape and waiting for the government approval.

Physics and background conditions set stringent requirements on the SuperB Layer0: thickness, readout speed, segmentation, radiation resistance.

Technology options for SuperB Layer0 under study → DNW MAPS, hybrid pixel + vertical integration.

A first DNW MAPS matrix with in-pixel sparsification and timestamp information fully characterized and tested with beams:
   → very encouraging results: threshold dispersion of 60e-, estimated S/N =23.

A FE chip for hybrid pixel tested and ready to be bump bonded to the pixel sensor matrix → characterization starting on September.

Plan to exploit the vertical integration both for hybrid pixel (FE chip with 2 tiers) and DNW MAPS with an expected improvement of performances.
backup slides
Good progress in Back. Simulation

- Hit rate, Radiation Dose, equivalent fluency plots produced for all SVT layers. Machinery is now in place!
- Different beampipe & L0 configurations studied but rates in L0 still very high.
- Layer 0 with radius ~ 1.5 cm
  - Rate > 200 MHz/cm² !!!
  - TID > 30 Mrad/yr !!!

Background dominated by $e^+ e^-$ pair production
Rate of low momentum $e^+ e^-$ hitting the beam pipe and Layer0 can be reduced increasing the B field ... need to investigate carefully this option.
Machine backgrounds

- Two colliding beams
  - radiative Bhabha → dominant effect on lifetime
  - e+e- e+e- production → ~3% contribution to lifetime, important source for SVT layer-0

- Single beam
  - synchrotron radiation → strictly connected to IR design
  - Touschek → negligible in BaBar, important in SuperB
  - beam-gas
  - intra-beam scattering

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<thead>
<tr>
<th>Beam Strahlung</th>
<th>Cross section</th>
<th>Evt/bunch&lt;sub&gt;xing&lt;/sub&gt;</th>
<th>Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>~ 340 mbarn</td>
<td>~680</td>
<td>0.3THz</td>
<td></td>
</tr>
<tr>
<td>(E&lt;sub&gt;γ&lt;/sub&gt;/E&lt;sub&gt;beam&lt;/sub&gt; &gt; 1%)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>~ 40 mbarn</td>
<td>~80</td>
<td>35GHz</td>
<td></td>
</tr>
<tr>
<td>(E&lt;sub&gt;γ&lt;/sub&gt;/E&lt;sub&gt;beam&lt;/sub&gt; ≥ 50%)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pair production</td>
<td>~7.3 mbarn</td>
<td>~15</td>
<td>7GHz</td>
</tr>
<tr>
<td>Elastic Bhabha</td>
<td>O(10&lt;sup&gt;-4&lt;/sup&gt;) mbarn (Det. acceptance)</td>
<td>~200/Million</td>
<td>100KHz</td>
</tr>
<tr>
<td>Y (4S)</td>
<td>O(10&lt;sup&gt;-6&lt;/sup&gt;) mbarn</td>
<td>~2/Million</td>
<td>1 KHz</td>
</tr>
</tbody>
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Background rates

- **Pair production**
  - Low $P_t$ make magnetic shielding effective
  - Issue for first layer of SVT
  - Rate $15\text{MHz/cm}^2$ @ 1.2 cm
    $5\text{MHz/cm}^2$ @ 1.5 cm

- **Radiative Bhabhas**
  - Beamline and shielding esse buak
  - Showering and backscattering extends to large radius
  - Rate $100\text{kHz/cm}^2$ @ R=1.2 cm

- **Touschek Background**
  - Produced all along the ring, depending on emittance and bunch volume
  - Beam optics and collimator setting essential in controlling this background
  - Rate $<10\text{kHz/cm}^2$ @ R=1.2 cm
New MAPS testbeam in July 2009

Results for MAPS (3x3 matrix) with analog output (pre/post irradiation 10 Mrad)

- Qcluster ~1040 e- for M1 (930 e- for M2)
- S/N~15-20 depending on the electrode geometry
- Efficiency~90% for both M1,2 @400e- in agreement with the measurements on digital MAPS
- Modest reduction in collected charge and efficiency in chip irradiated up to 10 Mrad
  - S/N reduction due to the increase of ENC. (30-40%)
Radiation tolerance of DNW MAPS

- Irradiation with $^{60}$Co $\gamma$-ray up to $\sim$ 10 Mrad
- Gain reduction $\sim$ 3%/MRad
- Noise increase $\sim$ 15%/MRad
- Significant recovery after 100ºC/168h annealing cycle
  - Noise increase $\sim$ +33% @ 10 MRad
- Charge collection efficiency under test
- Next step investigate bulk damage
The total radiation length of this module is $0.28 \% X_0$.

An internal peek tube 50 $\mu$m thick is used to avoid moisture on carbon fiber.
Epoxy glue used to place microtube on very thin transversal CfRP stiffeners.

Micropositioning and microgluing work required a dedicated gluing mask!

Sealing of the hydraulic interface obtained with epoxy/CFRP.

The Net Module has the same hydraulic parameter/microtube, already measured for Microchannel module.
Full Module Test Results

Temperature along the module (\(\Delta T = 5 \; ^\circ\text{C}\) )