Fast Tracker: A Hardware Real Time Track Finder for the ATLAS Trigger System

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Introduction

- Fast Tracker (FTK) : on-line hardware tracking system for ATLAS upgrade.

- FTK reconstructs all track with PT>1 GeV/c for Level 1 accepted events and provide track information at the beginning of level 2 trigger processing.

- Track information makes it possible to implement more efficient and complex trigger algorithms at Level2.

- Extremely difficult task 25 ns inter-bunch space and ~70 pile-up in highest luminosity run.
The FTK basic ideas (1)

Pattern Recognition

- The most probable $10^9$ patterns are pre-computed and stored in the Pattern Bank.
  - Pattern matching at limited resolution to reduce the number of required patterns.

- Thanks to the Associative Memory feature all the hits in each event are compared simultaneously with all the patterns in the Bank and track candidates are found.

Pattern recognition is complete when the hits have been transferred off the detector.

Very fast pattern reconstruction!
Associative memory Chip

Pattern bank is stored to Associative Memory (AM) Chip.

**New version AM Chip:**
- ASIC 65 nm technology instead of 180 nm
- **128 k patterns / Chip** instead of 5 k
- Die size: 12 x 12 mm²
- Clock frequency 100 MHz
- CAM-like “don’t care” capability to have *variable resolution pattern width* to optimize efficiency, pattern density and noise rejection

**Patterns:**
- **Thin pattern**
- **Wide pattern**
- **Variable resolution pattern**

: Hit on track
💥 : Fake hit
--- : Track

Pattern for all tracks:
- 3 patterns, no fake
- 1 pattern, Fake hits match as pattern
- **1 pattern, no fake**

Last 2 bits of hit position are “don’t care” bits
The FTK basic ideas (2)

Track Fitting

- Track Parameters are calculated by linear approximation using full resolution hit coordinates for all the combination in each pattern.
- Constants are pre-computed for each of the 5 track parameters and the $\chi^2$ components using MC simulation.
- Reducing the fits to scalar products can be performed at high speed in FPGA (~1 fit/ns).

Example of Truth Tracks

**Track Parameters:**
- $P_T$, $d0$, $z0$, $\text{eta}$, $\text{phi}$

$$\tilde{p}_i = \sum_{l=1}^{N} C_{il}x_l + q_i$$

Track Fitting allows fast reconstruction of track parameters using full resolution hits.
FTK System

FTK system is highly parallelized to reconstruct tracks at the full 100 kHz level-1 accept rate using data received from whole ATLAS silicon detector.

64 regions -> 128 PUs -> 512 pipelines -> 8192 AM chips
FTK latency

<Z -> µµ, L=3x10^{34} \text{ cm}^{-2} \text{s}^{-1}, \text{pile up} \sim 69 \text{sample}>

Emulated results of FTK execution time using 69 pile-up sample. Dense events increase latency, but after few events the execution time quickly returns to the typical range.

L=3x10^{34} MC sample (Z->mm)

FTK can provide all tracks on average in ~40 micro sec. It is fast enough for HLT trigger inputs.
FTK Performance (Track Efficiency)

Efficiency with respect to offline

- FTK tracks have more than 90% efficiency with respect to offline tracks.
- Small inefficiency is basically due to the geometric coverage of the pattern banks and tighter requirement of hits existence.
FTK Performance (Track Resolution)

FTK and Offline tracks have similar resolution.
Object performance (B-tag)

FTK Barrel (eta<1.1)

It is the baseline of FTK!

- FTK and Offline have similar d0 distribution.
- Performance does not degrade in high pile-up.
- Example: Offline 70% Eff b-tag working point, 85% trigger Efficiency, w L2 Rejection 5
Primary Vertex Finding

- FTK full tracking allow primary vertex finding at every Level -1 accept.
- Standard online vertex finding on FTK Tracks.
- There is good linear correlation with both the number of offline vertices and the number of interactions.

Vertex Z Position resolution by vertex fitting is $56\mu m$. 
Tau Trigger

- FTK tracks have Level2 algorithm track level quality.
- Cone size can be identical to that used offline.
- With FTK tracks, there is more time for an offline-like tau identification algorithm in the trigger.
Status of hardware development
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- All board prototypes are progressing well.
- Board prototypes can be tested in the Vertical Slice at CERN.
Installation Schedule

- Prototypes available in 2013
  - AM chip06 late 2014
- Integration mid 2014 before production
- Installation and commissioning
  - 8-16 PUs June 2015 covering the central rapidity region.
  - Test with beam before production
- 32 PUs for full coverage up to ~50 pile up (2016)
- Expand to the full system (128 PUs) as needed by the luminosity profile.
Summary

• FTK provides full tracking information at offline quality for track above 1 GeV/c in time for Level 2 trigger.

• Current results are preliminary. IBL effect will be studied soon. Promising results are counted on.

• Development is going smoothly. we will start installation in 2014 and we will start data taking in a restricted rapidity region in 2015.

• Fast TracKer (FTK) Technical Design Report: [CERN-LHCC-2013-007 ; ATLAS-TDR-021]