CHAPTER 1

Introduction

1.1. The Problem of Triggering in High Energy Physics

In high-energy physics experiments the detectors generate big amount of data at a quite high rate. For example at LHC a bunch crossing frequency of 40 MHz generates a burst every 25 ns. These data can not be saved on-line since it would require a too huge and fast memory. On the other hand most of these data are considered as background and, consequently, must be somehow rejected. This is why a fast and dedicated electronics is required. The main job of the device, here in after called trigger device, is to select on-line the possible data from the background noise. It should be noted that the trigger device absolutely must not reject any significant event and, in case of doubt, must save it. This task is generally divided into several stages and the electronics is named trigger device of I, II, III level and so on. At LHC the I level trigger job requires approximately 3 μs to carry out a first on-line selection of incoming data. For this reason the data are temporarily stored inside a FIFO while, at the same time, are analyzed with a pipelined architecture that, in case of data validation, after 3 μs, transfers the stored data to the II level trigger device. This is shown in Figure 1.1.

The I level trigger can be designed by means of both programmable and ASIC logic depending on several trade-off. For example, the electronics for the I level trigger generally is very close to the detector and, consequently, its performances may be affected by radiation. Obviously the components should be as much radiation tolerant as possible but no component is granted to be radiation hard for high radiation and long exposure time. It can be said that, at a given radiation power and exposure time, the programmable devices are less radiation tolerant than ASICs due to their internal memories. In fact, radiation can induce latch-up effects on CMOS transistors, can flip digital devices or even permanently damage the silicon. Nevertheless, apart from the permanent damages, the programmable devices can work in a completely different way they were designed for. In fact, if a digital flip occurs on the internal configuration memory, the programmable device can completely change its performance. On the other hand, ASICs, at most may be forced into changing some internal levels that hopefully should not affect seriously the global performance. For this reason ASICs are more radiation tolerant than programmable devices.

Anyway the choice among the available electronic devices is also based on the cost, since several thousands of components must often work in parallel on different sets of data. From this point of view ASICs, especially for many thousands of pieces, become much cheaper than programmable devices.

Finally, taking into account that with FPGA implementation it is possible to reach prototype preliminary results in shorter times, it may be accepted as a rule of thumb to apply firstly an FPGA and, lately, the same architectures may be applied and implemented with Application Specific Integrated Circuits (ASICs).

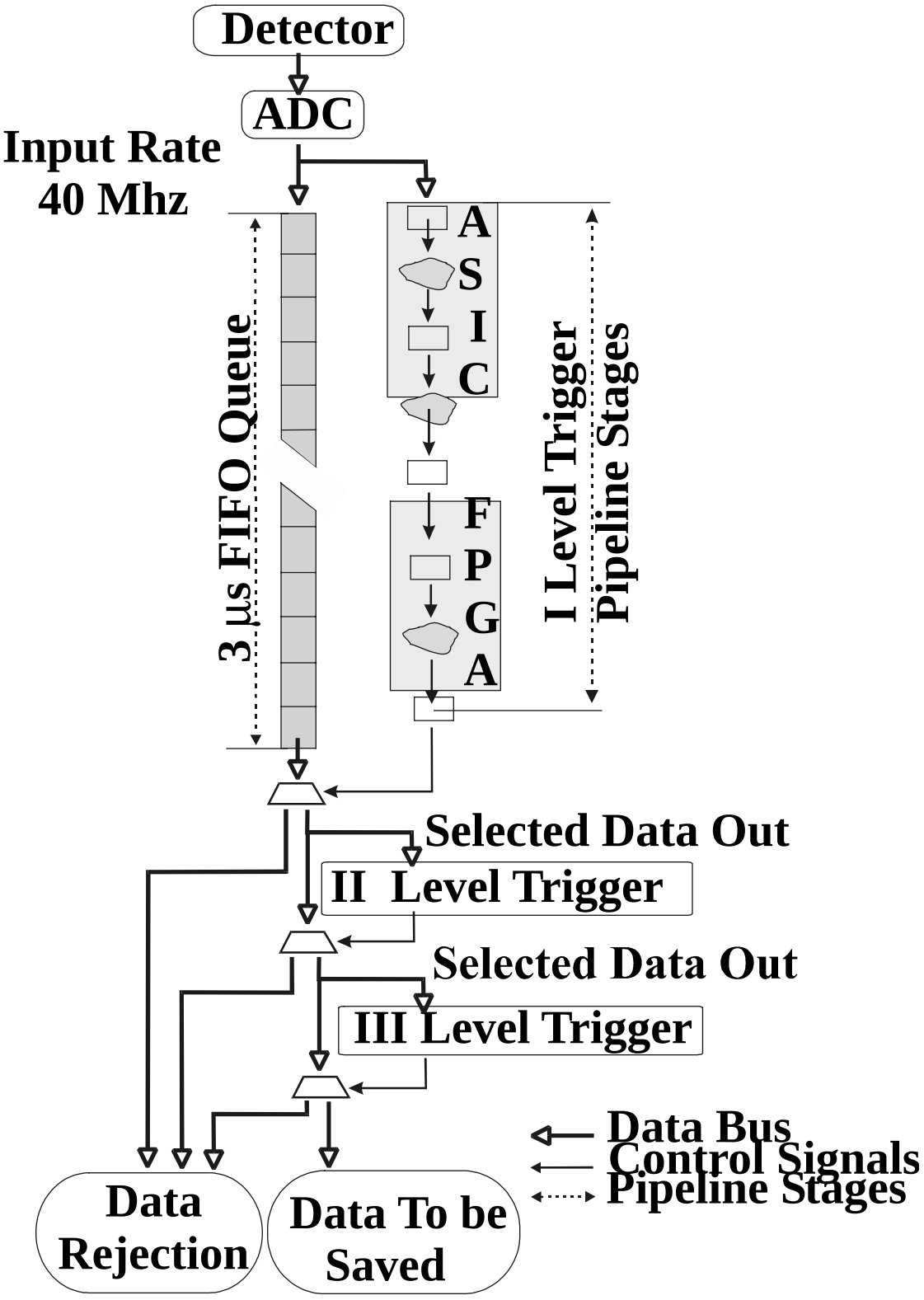

Figure 1.1. Trigger sketch

Besides that, there are also hybrid devices such as only-once Programmable Application Specific Integrated Circuits (PASICs) that merge the flexibility of programmable devices and the performances of ASICs, once again in despite of costs.

In Figure 1.1. it is shown a First In First Out (FIFO) architecture that takes the functions of a queue for the incoming data. While data are stored into the FIFO the I level trigger analyzes the data with a pipeline structure that, for example, is composed first by an ASIC and then by an FPGA. At the end of the pipeline stages a control signal forces a multiplexer into transferring the previously stored data to the II level trigger or to the waste. Thus the II level trigger, that receives data at an average rate of some tens of kHz, has a longer time for making a second level selection. In the same way works the III level trigger that receives data at about 100 Hz rate.

Of course the longer is the time available by the trigger level the more refined can be the data selection. For example the selection can take care of some trajectories that have to be identified, or some signal levels that have to overcome a given threshold.

1.2. Fuzzy Logic Applications for High Energy Physics

In some particular application fields, where high computation performances are required, fuzzy processors can be applied and implemented on electronic boards and systems [1], [2]. In other words, for some dedicated application fields where traditional processors require a well-defined input-output algorithm, fuzzy processors may be trained just with input training patterns. Nowadays, for this aim there are many methods for training a fuzzy system: again fuzzy rule based systems, neural network based systems, genetic algorithm based systems, hybrid systems among the latter ones and so on. Nevertheless, the fuzzy system can solve a problem independently of knowledge of the input-output relationship. For this reason it has been investigated the possibility to implement high-speed fuzzy processors for high-energy applications. For example, where the input-output relationship of a given function is not easily found, fuzzy logic may be adapted and applied. From another point of view fuzzy logic, once implemented into dedicated hardware, can solve much more quickly the same problems that traditional logic does slower. This leads to possible applications to HEPE trigger problems.

In this application fields in fact, the electronic devices used for detecting, recognizing and saving physics events must be as fast as possible, and have to be designed with a high noise immunity, low power consumption and high performances in terms of reliability, robustness and flexibility. These features have been met both by applying a parallel-pipeline architecture and by implementing a no-time consumption rule identification within the fuzzy processors.

1.3. Technological Implementation

As far as the technological implementation of the designs presented in this thesis, the Complementary Metal Oxide Semiconductor (CMOS) Very Large Scale Integration (VLSI) digital technology fits very well our preliminary constraints. The digital technologies have been chosen instead of analog one since they let the designers use standard cells. With these cells a digital electronics designer feels much more confident than an analog one and has the possibility to design larger and more complex

architectures. In fact, apart from fabrication bugs, the digital prototypes have themselves very good chances to work properly. In other words a designer, before starting a work, has to select a given technology not only depending on his/her constraints but also depending on the designing methodology: digital based on standard cells, full custom digital, full custom analog, hybrid and so on. We have chosen the first for the previous reasons. Full custom digital design means that one has to design his/her own the basic logic ports, flip flops and so on. This can be seen as a further degree of freedom but can really give some advantages only if one needs very constrained cells. In all the other cases, the large majority, the wide cell availability is enough for most projects. Indeed, the cells developed by a silicon foundry have had a huge and deep worldwide test over prototypes before being delivered. This is why they give confidence to the designers.

Full custom analog designing (there is no standard-cell-based analog one), the latter problem is even bigger. Moreover the presented designs have been made with the technical support of IMEC microelectronics center in Leuven – Belgium. This particularly applies for ASIC designs. The design of the fuzzy processors have been done using VHDL language, they are cell-based and have been implemented with 0.7 μm CMOS VLSI technology.

1.4. Chapters Presentation

This thesis mainly deals with prototype processor and architecture designs for High Energy Physics Experiments (HEPE). Particularly the design and development have been done for applications to trigger devices for Istituto Nazionale di Fisica Nucleare (INFN) experiments. For example, the first part of this research (Chapter 2) focuses on the design and realization of a fast electronics architecture able to make a decision in a very short time; say a few hundreds of ns. This was investigated for possible applications on I or II level trigger devices. In order to meet the speed constraints fuzzy logic has been applied since it is well known that in some given dedicated fields it may give rise to several advantages. Thus, firstly it has been designed and realized a 4-input 7-bit fuzzy processor able to carry out computations within 320 ns for a 50 MHz clock signal. This fast digital Fuzzy Processor has already been designed and realized in 0.7 μm digital CMOS technology obtained by European Silicon Structure (ES2) silicon foundry. It processes four 7-bit input variables and carries out one 7-bit output one. It may be synchronized up to a 50 MHz clock signal for an estimated power consumption of nearly 1300 mW. Moreover the input/output delay of this chip varies from 80 ns to 320 ns depending on the number of input variables. This has been a preliminary research that, in case of application, could be improved by means of even faster technologies for matching the I or II level trigger requested speed.

In the processor the innovative idea is the no-time consuming methodology for selecting the *fuzzy active rules*. This is done by a parallel-pipeline architecture described in details. In the section are summarized the Fuzzy Processor future implementations for HEPE. In addition, the architecture is explained with layout and data flow simulation pictures. Moreover the fuzzy logic methodologies which have been adopted are justified in terms of hardware implementation feasibility and speed requirements. This research was included into the V technological research group of INFN.

Secondly, once again in the framework of research, another 2-input fuzzy processor has been designed and realized for improving the processing time of the first processor up to a few tens of ns despite of the number of inputs that have been set to 2.

Chapter 3 deals with the design and the realization of a small-size high-speed digital fuzzy processor that is aimed to improve and give more flexibility to the front-end electronics of HEPE. We think that the high processing time of the processor (80 ns) could extend its applications in many other fields.

On the other hand, for the Large Hadron Collider (LHC) an electronic prototype board has been developed for the A Large Ion Collider Experiment (ALICE). This is described in detail in the fourth chapter where a Field Programmable Gate Array (FPGA) has been applied as a programmable device. This part of research has been made in collaboration with the Torino section of INFN. This prototype board is described in Chapter 4.

In the Appendix 1 are reported the VHDL codes of the fuzzy processor described in Chapter 1