2D and 3D Thin Pixel Technologies for the Layer0 of the SuperB Silicon Vertex Tracker

F. Giorgi

INFN and University of Bologna

On behalf of the SuperB SVT collaboration
Outline

• The SuperB project
• The Silicon Vertex Tracker (SVT)
• TDR layer0 options
  – Baseline
  – Pixel upgrade
• Investigated Pixel Technologies
• Lab and beam tests results
• New digital readout architecture.
• Conclusions and perspectives
The SuperB project

- Flavour physics promises sensitivity to New Physics ... but **large statistics is needed** (50-100 ab\(^{-1}\))
- An upgrade to the first generation of B-Factories (PEP-II and KEKB) of \(\sim 2\) **orders of magnitude** in \(\mathcal{L}\) is needed to get **50 ab\(^{-1}\)**.
- The **SuperB** factory is an Italian e\(^+\) e\(^-\) accelerator concept that allows to reach \(\mathcal{L}=10^{36} \text{ cm}^{-2} \text{ s}^{-1}\) with **moderate beam current** (2A) using very **small beam size** (~1/100 of present B-Factories beams).
- **2007**: Conceptual Design Report published
- **2010**: Approved by the Italian Government (250 ME allocated for the Infrastructures)
- **2011**: Established site: Roma Tor Vergata
- Management under **Cabibbo Lab** consortium (INFN, Uni Tor Vergata, IIT).

**Next steps:**
- Spring 2012: Technical Design Report
- Mid 2016: 1\(^{st}\) collisions.
Silicon Vertex Tracker

**B → π π decay mode, βγ=0.28, beam pipe X/X₀=0.42%, hit resolution =10 μm**

**Layer0**

**Design based on the 5-layer Babar SVT (R>3cm)**

**BUT:**

1) Due to reduced beam **energy asymmetry** (7x4 GeV vs. 9x3.1 GeV) required an **improved vertex resolution (~factor 2)**
   - EXTRA Layer0 very close to IP (@1.5 cm) with **low material budget** (<1% X₀) and **fine granularity** (50 μm pitch)
   - Layer0 area 100 cm²

2) Bkg levels depend steeply on radius
   - Layer0 needs to be **fast and rad hard** (>20x5 MHz/cm², >3x5 MRad/yr)
Silicon Vertex Tracker

• **Baseline**
  – 5 layers of *silicon strip* modules (extended coverage w.r.t BaBar)
  – **Striplets** for layer0 @ R~1.5 cm
    • Fast readout chip, ongoing R&D.

• **Layer0 upgrade** for full luminosity run
  – SVT Mechanics will allow a *quick access/removal* of Layer0
  – Upgrading to thin *pixel sensors*
    • **More robust** against background occupancy
    • Several options investigated:
      – **CMOS MAPS**: Continue R&D on *readout speed* and *rad hardness*.
      – **Hybrid Pixels**: FE chip development *50x50 um pitch* with *fast readout* and
        R&D on reduction of total module *material* below 1% $X_0$.
      – **Vertical Integration**: can we access this technology on time in a *reliable*
        and *stable* way?
  – R&D continue in 2012 after TDR ⇒ pixel technology decision by 2013
**Pixel technologies under study**

**Deep N-well MAPS,**
- **In-pixel** front-end electronics (pre, shap, discr).
- **competitive N-well** issue

**3D MAPS**
- **Separated digital tier:** dense pixel digital logic and peripheral readout
- **In-pixel** analog FE
- **Less competitive N-well issue**

**INMAPS technology**
- Deep P-well **preventing charge-stealing** by competitive N-wells.
- High resistivity substrate → more robust against radiation.

**Hybrid Pixels 50x50 um pitch**
- High resistivity, **fully depleted sensor**
- **Fast readout** (analog FE and digital logic at pixel level)

**FUTURE... 3D front-end chip**
- Dedicated **digital tier**
- **analog tier:** FE electronics.
- **Fully depleted detector** Bump Bonded / Directly Bonded

**APSEL4D chip**
- **ST 0.13 um**
- Beam test CERN 2008.
  - 90% efficiency compatible with deep N-well fill factor

**APSEL3D**
- Tezzaron Chartered
- 32x8 matrix with Digital readout. Ongoing tests

**INMAPS 0.18 um**
- 32x32 matrix submitted June 2011

**SuperPix0 chip**
- Beam Test Sept. 2011.
- Preliminary results presented
Tezzaron Chartered 3D MAPS: APSEL5T

- **2D structures** (analog tier only) had been tested, encouraging results
- ENC ~ 45 e-
- Preliminary estimate of MIP signal from test Sr90 ~ 850 e-
- **Beam test** in the **end of Sept.**, ongoing analysis.

- **3D structures** (analog + digital) **just arrived**. Currently under test. We observed some problems that must be understood.

2 other Chartered/Tezzaron submissions are foreseen after the 1st run characterization is complete.

*(New Readout Architecture* same as INMAPS submission)*

- **MAPS 3D** chip APSELVI (128x96)
- **3D FE** chip for hybrid pixel **Superpix1** (32x128) 50 um pitch
Hybrid chip SuperPix0 lab tests

High thresholds (1/2 MIP) scan: Response to $^{90}\text{Sr}$
Good bump bonding: few defects over 5 chips (~ $2.10^{-4}$)

5 detectors tested
- Mean ENC 78 e-
- Fully Sensor SNR : 200
- Thr. Dispersion 520 e- (No thresholds fine adjustments, but foreseen for next chip)

→ Phys. Runs with thresholds at 1/4 MIP due to high thr. dispersion.

Some pixels occupancy VS threshold
SuperPix0 Beam Test

End of Sept. 2011, CERN SPS north area - 120 GeV pions

- Preliminary results (analysis started 3 weeks ago)
- Resolution compatible with pitch (50 um)/√12
- Efficiency 98.5 % at 1/4 MIP and 1/8 MIP

Due to known induction problem, the chip was operated in atypical conditions that could affect the efficiency. Quantification in progress.

Preliminary efficiency vs threshold graph:

1/4 M.I.P.

Setup
- Telescope: 6 layers of double sided silicon strip
- 2 DUTs
- Motorized support

DAQ Boards
- 16 FE channels
- 2x 1.3 Gbps
- Optical links
- 120 kHz peak evt. rate
New Pixel Readout Architecture Features

- **In-pixel** Hit & Time Stamp Latch
- **TS request** to the matrix
- Pixel FastOR activates **IF** latched TS == requested TS
- Cascaded column FastORs
- **Only active-FastOR columns are enabled in sequence.** (i.e. 10 active column FastORs → 10 clk cycles readout)
- **Each column sparsified in 1 clk cycle** (whatever the occupancy)
- **Triggered** and **Data-Push** mode.
- **Implemented** in our last INMAPS submission & ready for next 3D submissions

**Specifications**

- **130 MHz hit rate.**
- **192x256 matrix**
- **50 MHz read clock**
- **2.5 MHz trigger rate (stressed condition)**
- **200k events** per point

**Simulations**

DO NOT take into account:
- Sensor Efficiency.
- Analog FE.

**Graphs**

- **TRIGGERED MODE**
  - Pixel latches as latency buffers
  - **98.2% efficiency**

- **DATA PUSH MODE**
  - **130 MHz hit rate.**
Conclusions and Perspectives

• **SuperB machine approved.**
• **TDR by spring 2012**
• Foreseen SVT layer 0 **upgrade** for full luminosity

Several technology options under study:

– Hybrid Pixel, **low pitch** and **fast readout**, high **threshold dispersion**
  →fine threshold adjust at pixel level.
– Encouraging results from 3D MAPS analog tier APSEL_5T **ENC 48 e-**
– 3D structures just arrived, lab tests ongoing.
– INMAPS process just submitted.

• **Next year To Do list:**
  – Wide matrix 3D MAPS & 3D FE chip
  – INMAPS chip and 3D structures on beam
Thank You

The SuperB SVT Collaboration

C. Avanzini\textsuperscript{a}, G. Batignani\textsuperscript{a}, S. Bettarini\textsuperscript{a}, F. Bosi\textsuperscript{a}, G. Calderini\textsuperscript{a}, G. Casarosa\textsuperscript{a}, M. Ceccanti\textsuperscript{a}, R. Cenci\textsuperscript{a}, A. Cervelli\textsuperscript{a}, F. Crescioli\textsuperscript{a}, M. Dell'Orso\textsuperscript{a}, F. Forti\textsuperscript{a}, P. Giannetti\textsuperscript{a}, M.A. Giorgi\textsuperscript{a}, A. Lusiani\textsuperscript{b}, S. Gregucci\textsuperscript{a}, P. Mammini\textsuperscript{a}, G. Marchiori\textsuperscript{a}, M. Massa\textsuperscript{a}, F. Morsani\textsuperscript{a}, N. Neri\textsuperscript{a}, E. Paoloni\textsuperscript{a}, M. Piendibene\textsuperscript{a}, A. Profeti\textsuperscript{a}, G. Rizzo\textsuperscript{a}, L. Sartori\textsuperscript{a}, J. Walsh\textsuperscript{a}, E. Yurtsev\textsuperscript{a}, M. Manghisoni\textsuperscript{c}, V. Re\textsuperscript{c}, G. Traversi\textsuperscript{c}, M. Bruschi\textsuperscript{d}, R. Di Sipio\textsuperscript{d}, B. Giacobbe\textsuperscript{d}, A. Gabrielli\textsuperscript{d}, F. Giorgi\textsuperscript{d}, G. Pellegrini\textsuperscript{d}, C. Sbarra\textsuperscript{d}, N. Semprini\textsuperscript{d}, R. Spighi\textsuperscript{d}, S. Valentinetti\textsuperscript{d}, M. Villa\textsuperscript{d}, A. Zoccoli\textsuperscript{d}, M. Citterio\textsuperscript{e}, V. Liberali\textsuperscript{e}, A. Stabile\textsuperscript{e}, F. Palombo\textsuperscript{e}, L. Gaioni\textsuperscript{f}, A. Manazza\textsuperscript{f}, L. Ratti\textsuperscript{f}, V. Speziali\textsuperscript{f}, S. Zucca\textsuperscript{f}, D. Gamba\textsuperscript{g}, G. Giraudo\textsuperscript{g}, P. Merew\textsuperscript{g}, G.F. Dalla Betta\textsuperscript{h}, G. Soncini\textsuperscript{h}, G. Fontana\textsuperscript{h}, M. Bomben\textsuperscript{i}, L. Bosisio\textsuperscript{i}, P. Cristaudo\textsuperscript{i}, D. Jugovaz\textsuperscript{i}, L. Lanceri\textsuperscript{i}, I. Rashevskaya\textsuperscript{i}, L. Vitale\textsuperscript{i}, G. Venier\textsuperscript{i}

(a) Universita degli Studi di Pisa and INFN-Pisa, Italy
(b) Scuola Normale Superiore and INFN-Pisa, Italy.
(c) Universita degli Studi di Bergamo and INFN-Pavia, Italy.
(d) Universita degli Studi di Bologna and INFN-Bologna, Italy.
(e) Universita degli Studi di Milano and INFN-Milano, Italy.
(f) Universita degli Studi di Pavia and INFN-Pavia, Italy.
(g) Universita degli Studi di Torino and INFN-Torino, Italy.
(h) Universita degli Studi di Trento and INFN-Padova, Italy.
(i) Universita degli Studi di Trieste and INFN-Trieste, Italy.
Backup – Deep N-well MAPS
Backup Deep P-well INMAPS process

Fig. 2. Illustration of the depletion region width (pink) versus resistivity. From left to right: standard resistivity silicon, higher resistivity silicon, full depletion of epitaxial layer (ideal case). The deep p-well implant is also shown underneath the PMOS transistors, preventing charge from being collected by the n-wells in which they are situated.
R&D on pixel for Layer0 upgrade

MAPS radiation hardness: charge collection studied after neutron irradiation up to ~ \(7 \times 10^{12} \text{n/cm}^2\)

~ eq. to 1 yr in Layer0 (no safety included!)

Noise and gain not affected by neutron

Signal degradation after each irradiation step studied with \(\beta \text{ Sr}^{90}\) source:

- SNR \(\rightarrow\) 10 in last step
- severe limitation for application in Layer0

Investigating INMAPS process (180 nm):

high-\(\Omega\) epilayer available for improved charge collection and radiation hardness!

4th well (deep Pwell), below nwells for in-pixel logic, is used to avoid charge stealing by competitors with sensing electrode.

same readout architecture optimized for 3D (more in-pixel logic thanks to 4\(^{\text{th}}\) well)

Summer 2011: submitted 32x32 matrix with digital readout and 3x3 analog structures.
Effects on equivalent noise charge

\[ ENC^2 = C_T^2 A_1 S_{ws,in} \frac{1}{t_p} + C_T^2 A_2 A_{f,in} t_p^{\alpha_{fn}^{-1}} + A_3 S_{wp,F} t_p + A_3 S_{wp,\text{leak}} t_p \]

- Channel thermal noise in the input device
- Flicker noise in the input device
- Parallel noise in the feedback MOSFET
- Parallel noise in the detector leakage

DNW-MAPS (900 \( \mu \text{m}^2 \) area)

- Red circles: before irradiation - measured
- Blue squares: 1100 krad - measured
- Orange triangles: after annealing - measured

Affected by ionizing radiation.
Radiation tolerance of DNW MAPS

- Irradiation with $^{60}$Co γ-ray up to ~ 10 Mrad
- Gain reduction ~ 3%/MRad
- Noise increase ~ 15%/MRad
- Significant recovery after 100°C/168h annealing cycle
  - Noise increase ~ +33% @ 10 MRad
- Charge collection efficiency under test
- Next step investigate bulk damage

Apsel3T1 test chip ($t_p=200, 400$ ns)

ENC [e- rms] vs Dose [Mrad]

Charge sensitivity [mV/fC] vs Dose [Mrad]
Results on Superpix0

Gain (by $C_{\text{inj}}$ scans):
- 38.0 mVfC with sensor (6% dispersion), 40.9 mV/fC w/o sensor (5%)

Noise ($\text{ENC} = \text{RMS}_{\text{noise}}/\text{Gain}$):
- 66 e- w/o sensor, 81 e- with sensor $\Rightarrow S/N = 200!$

Threshold dispersion ($\text{RMS}_{\text{baseline}}/\text{Gain}$):
- 478 e- w/o sensor - 482 e- with sensor
- Pixel threshold tuning circuit implemented in the next design

Response to a Sr90 source (e-)
$\rightarrow$ good quality of the interconnection @ 50x50 $\mu$m² pitch & working sensor!!

CHIP12: all ch. working

CHIP19

5 defects on 2 chips
$6 \times 10^{-4}$

pixels not working

pixel not connected to the sensor

source shifted to the right

due to known problem on the FE chip
In the active sensor area we minimized:
- logical blocks with PMOS to reduce the area of competitive n-wells
- digital lines for point to point connections to allow scalability of the architecture with matrix dimensions

$4K(32 \times 128)$ 50x50 μm$^2$ matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:
- Register hit MP & store timestamp
- Enable MP readout
- Receive, sparsify, format data to output bus

S/N ~ 20 with power consumption ~ 30 μW/ch

Signal for MIP (MPV) = 980e-

Landau mV

Cluster signal (mV)

Threshold dispersion = 60 e-

Gain = 860 mV/fC
DNW MAPS Hit Efficiency measured in a CERN beam test (APSEL4D)

Efficiency vs. threshold

Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

MAPS hit efficiency up to 92 % @ 400 e- thr.
300 and 100 µm thick chips give similar results
Intrinsic resolution ~ 14 µm compatible with digital readout.


Competitive N-wells (PMOS) in pixel cell steal charge reducing the hit efficiency: fill factor (DNW/tot N-well) ~ 90 %

2D MAPS: efficiency can improves adding multiple collecting electrodes around competitive nwells, even better using a quadruple well process (INMAPS being considered).

3D MAPS: (2 tiers for sensor&analog + digital) fill factor and efficiency can improves significantly.
SPX0 Gain X-check in Pisa

With Am241 source (10 mCi), 30 DAC-wide (1 DAC~0.3 mV) noise scan around the endpoint. Line-Fit for the extrapolation of the end-point of the spectrum.

Subtract the baseline (from noise scan) from the extrapolated abscissa and assume 60 keV as released energy (∴ 16 600 e-)

This method provides a biased (-10%) estimate of the gain!

The photo-electron of Fe55 has a range of ~1μm. Why don’t use that (~1/10MIP)?

We tried but ... we were sensitive to the baseline fluctuation due to T changes and the tiny signal was smeared in the long run.

\[ \frac{dV_{\text{base}}}{dT} \approx -1 \frac{mV}{^\circ C} \]