FSSR2, a Self-Triggered Low Noise Readout Chip for Silicon Strip Detectors

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***Abstract*– The FSSR2 is the second release of the Fermilab Silicon Strip Readout Chip. The chip has been designed and fabricated in a 0.25 μm CMOS technology for high radiation tolerance. The first release, simply called the FSSR, was a prototype version with many different analog front-end configurations. The best solution was chosen for the FSSR2 chip to optimize the noise, according to criteria discussed in this paper. The FSSR2 has been designed for the silicon strip detectors of the BTeV experiment. The chip services 128 strips and provides address, time and magnitude information for all hits. Several programmable features are included in FSSR2, such as an internal pulser, a baseline restorer and a signal peaking time selectable among four values in the range between 65 ns and 125 ns. The circuit design and the performance of FSSR2 are discussed in this paper.**

***Index Terms* —Front-end electronics, CMOS, Noise, silicon strip detectors**

I. Introduction

A FULL custom integrated circuit called the FSSR2 (Fermilab Silicon Strip Readout) chip has been designed and fabricated in the TSMC (Taiwan Semiconductor Manufacturing Company) 0.25 μm CMOS process to interface with silicon strip detectors and send digital information to the data acquisition system.

FSSR2 is the final step of an R&D effort which began with the design of the prototype chip FSSR [1]. The architecture of both FSSR and FSSR2 is a modified version of that of the FPIX2, the readout chip for the BTeV pixel detector [2]. FSSR2 has 128 analog channels, each consisting of a charge-sensitive preamplifier, a unipolar semigaussian shaper, a selectable baseline restorer (BLR), a hit discriminator and a 3-bit Flash analog-to-digital converter (ADC). The chip operates in a self-triggered mode with no analog storage.

The chip was designed for the readout of the Forward Silicon Tracker of the BTeV experiment at Fermilab. However, as discussed in the following, the performance of FSSR2 makes it suitable for a wide range of applications with microstrip detectors. Fig. 1 is a photo of the FSSR2 chip.

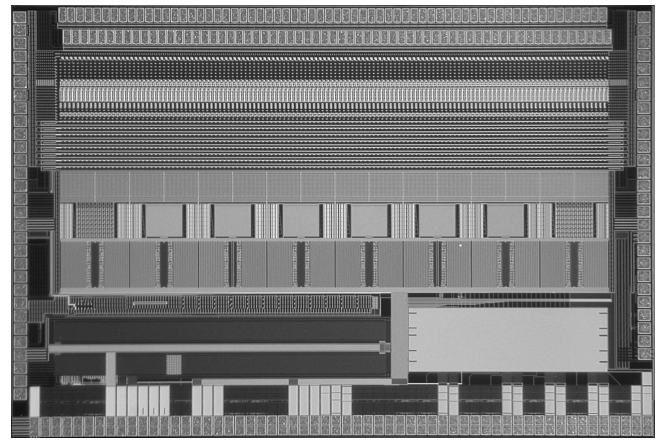

Fig. 1. Photograph of the FSSR2 chip with input pads at the top. The chip measures 7.5 mm x 5 mm and the input pads have an effective pitch of 50 μm.

II. Chip Description

A. Chip Specifications and FSSR2 Architecture

The FSSR2 chip can be considered as comprised of several parts, as shown in Fig. 2. The chip core consists of 128 analog channels, logically subdivided in 16 sets of 8 analog channels each, of the end-of-set logic (16 blocks, one for each set of front-end channels) and of the core logic, which controls the data flow from the core to the data output interface. If a hit is detected in one of the channels, the core transmits a 24-bit data word which carries information relevant to pulse amplitude, channel number and time stamp. A programming interface accepts commands and data from a serial input bus and programmable registers are used to hold input values for DACs that provide currents and voltages required by the core, such as the threshold level for the discriminators and the amplitude of the test signal generated by an internal pulser. The data output interface accepts data from the core, serializes the data and transmits them off chip on as many as 6 output LVDS lines, with a maximum data transmission rate of 840 Mb/s. The number of output lines is programmable, depending on the expected hit activity in the chip. The size of the strip sets was chosen in order for the readout architecture to handle a 2 % average strip signal occupancy at a bunch crossing period of 132 ns, with an efficiency greater than 99 %.

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As far as analog specifications are concerned, the analog channels were designed to achieve an Equivalent Noise Charge (ENC) smaller than 1000 e rms with a 20 pF detector capacitance C_D and a threshold dispersion across the chip smaller than 500 e rms. This allows for a low noise hit rate at a 0.2 MIP (Minimum Ionizing Particle) threshold setting. The power dissipation was held to less than 4 mW/channel.

Even if in an experiment like BTeV a simple binary output (Hit/No Hit) from each channel is sufficient for track reconstruction, in FSSR2 it was decided to include a low resolution ADC to calibrate the detector as radiation changes its characteristics.

The BTeV experiment set the requirement that the chip has to maintain its performance up to 5 Mrad total dose of ionizing radiation. To this purpose, enclosed geometry NMOS are used in the chip [3]. Specially designed registers are used to mitigate single event upset (SEU) problems. A discussion of these registers and measurement of their cross section are given in [4]. Since FSSR2 is a mixed signal design with very low noise requirements, care was taken to minimize noise coupling from the digital section to the analog section of the chip, as discussed in [1]. To this purpose, all digital pads use low voltage differential signals (LVDS).

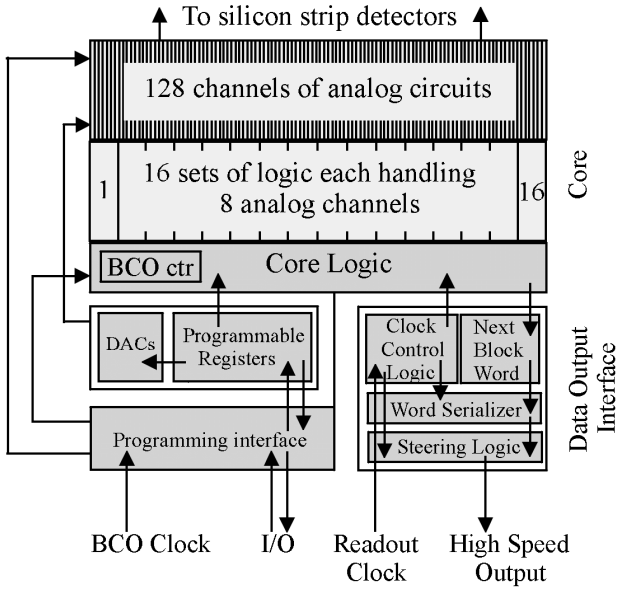

Fig. 2. Block diagram of the FSSR2 chip showing the core circuitry and the data output interface.

B. Analog Section

The schematic diagram of the analog channel in FSSR2 is shown in Fig. 3. The front-end stage consists of a charge-sensitive preamplifier, followed by a unipolar second order semigaussian shaper. In the preamplifier, a continuous reset is provided by a transconductor (with transconductance G_f). The shaping actually takes place in two steps. First the signal from the preamplifier undergoes an integration, then the shaping is completed by an active filter which provides one more integration and a differentiation and also implements a gain function. The signal peaking time t_P at the shaper output is selectable among four values (65 ns, 85 ns, 100 ns, 125 ns) by acting on capacitor values in the shaper [5]. This allows for good operation with different hit rates in the detector.

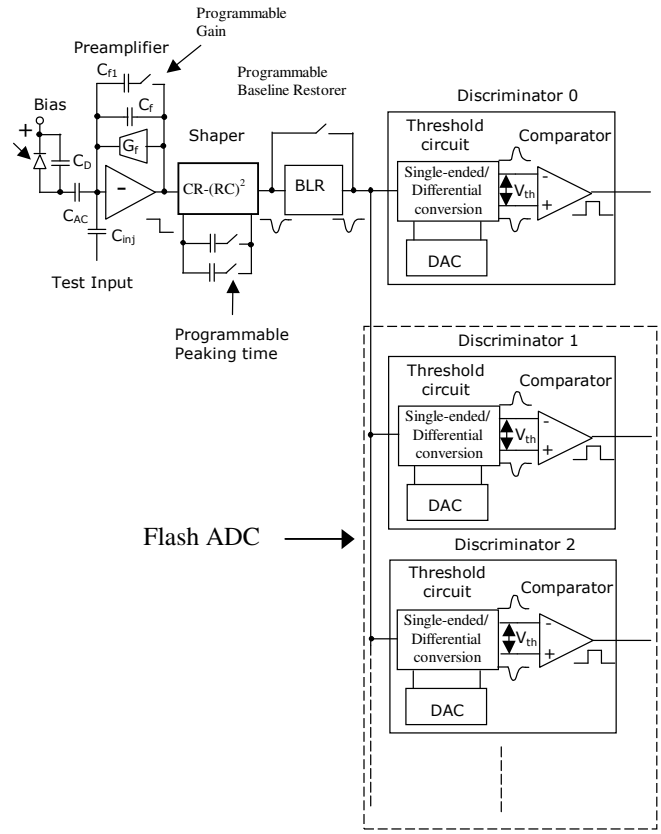

Fig. 3. Schematic of the analog channel in the FSSR2 chip. The DACs are shared by all 128 channels in the chip.

In the FSSR2, in the 128 channels the preamplifier input device is an NMOS with W/L = 1500/0.45 biased at a drain current I_D = 500 μA. The choice of the input device was made on the basis of noise measurements on the prototype and on noise optimization models for deep submicron technologies [6] - [9]. In the prototype FSSR, a number of test MOSFETs were added specifically to perform single device noise analysis. The characterization of single test devices yielded results such as those shown in Fig. 4. To comply with the specification on power dissipation, a constraint was set on the drain current, requiring I_D not to exceed 500 μA. The plot compares the noise voltage spectra measured at this I_D value for an NMOS with the same gate dimensions chosen as the preamplifier input device in FSSR2 and for a PMOS with a similar W/L ratio. The normalized transfer function of the semigaussian shaper in FSSR2 is superimposed to the plot to highlight the frequency region of interest at different peaking time settings. The plot shows that the peaks of the transfer functions always occur where white noise is dominant.

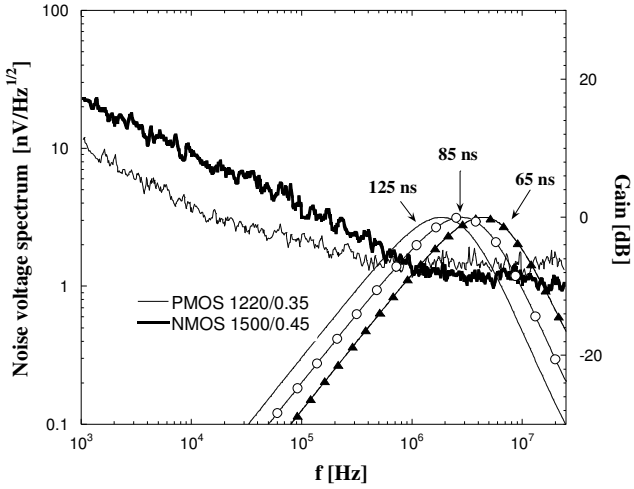

Fig. 4. Measured noise voltage spectra of a PMOSFET with W/L = 1220/0.35 and an NMOSFET with W/L = 1500/0.45 in the 0.25 μm process by TSMC at I_D = 500 μA. The normalized transfer function (from simulations) of the semigaussian shaper in FSSR2 is superimposed to highlight the frequency regions of interest at three peaking time settings from t_P = 65 ns to t_P = 125 ns.

Considering that noise optimisation has to be mostly based on the reduction of the white noise component, the analysis of the experimental results for the single devices in the 0.25 μm TSMC process shows that for both NMOS and PMOS devices a gate length larger than the minimum allowed by the technology avoids excess noise contributions. This conclusion is also valid for other deep submicron processes. Moreover, for a detector capacitance of 20 pF, a broad and shallow optimum value for the gate width is located between 1000 μm and 2000 μm.

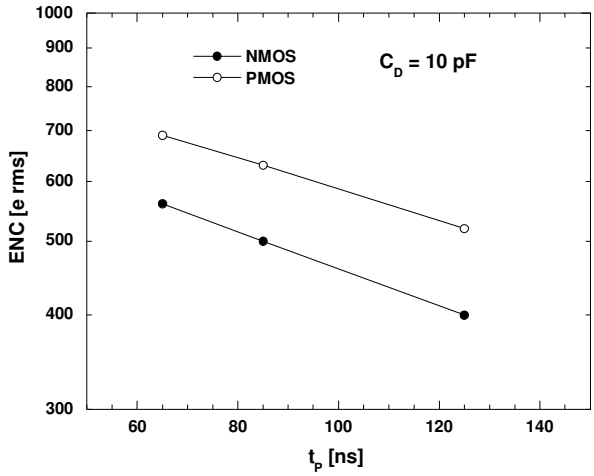

Fig. 5. Equivalent noise charge ENC as a function of the peaking time t_P at a detector capacitance C_D = 10 pF for analog channels in the FSSR prototype. The plot reports values measured on channels with an NMOS (W/L = 1500/0.45) and a PMOS (W/L = 1220/0.35) at the preamplifier input, both biased at I_D = 500 μA. Data are relevant to channels that did not include a baseline restorer.

The measurements on the single devices integrated in the prototype FSSR also show that the NMOS is preferable to the PMOS, as in Fig. 4, because of its smaller white noise contribution in the relevant peaking time range. In fact, at equal drain current, the PMOS is biased closer to strong inversion as compared to the NMOS, and therefore, it has a smaller transconductance [6], which results in a larger white noise. As shown by Fig. 5, this conclusion was confirmed by ENC measurements on analog channels integrated in the FSSR prototype, where the preamplifier input devices had the same gate dimensions as the NMOS and PMOS in Fig. 4. Restricting the choice to the NMOS, the better performance is achieved for a gate length close to 0.5 μm. The final choice of an NMOS with W = 1500 μm and L = 0.45 μm as the preamplifier input device allows for operation with good noise performance for detector capacitances in the range from 10 to 30 pF.

Several changes were made in the design of FSSR2 with respect to the prototype FSSR. First of all, the overall charge sensitivity G_Q was increased to reduce the discriminator threshold dispersion and meet the specifications with a good safety margin. Two nominal values of G_Q are selectable in FSSR2, 150 mV/fC and 100 mV/fC. The selection is achieved by acting on the preamplifier feedback capacitance, which can be increased from 100 fF to 150 fF (connecting the capacitor C_{f1} in parallel to C_f) to reduce the gain and increase the linear dynamic range. Secondly, after the shaper a baseline restorer can be used to cancel baseline shifts at the shaper output which affect the discriminator threshold. As shown in [1], a symmetric BLR is implemented according to the principles discussed in [10]. In FSSR2, the BLR is implemented in all channels in a programmable way, so that it may be used only when the strip signal occupancy is high. Limitations and advantages related to the BLR will be discussed in Section III. Finally, whereas the prototype FSSR provided only binary information concerning strip hits, in FSSR2 a 3-bit Flash ADC is implemented in each channel, giving analog information which may be used for detector monitoring and calibration. The discriminators in the ADC are driven by a threshold circuit, which converts the single-ended signal at the shaper output to a differential signal and superimposes a differential dc threshold voltage to the dynamic signal. A differential threshold voltage is used out of concern with crosstalk from the digital section on a single-ended threshold line. There is no threshold adjustment at the channel level: for all channels, the thresholds of the discriminators are set by DACs located in the programming interface. As shown by Fig. 3, discriminator 0 gives the binary information (Hit/NoHit). If it detects a hit, the 3 bit pulse amplitude information (generated by discriminators 1 to 7) for the relevant channel is attached to the output data word, as discussed in Section II-C. In FSSR2, 8-bit internal DACs are included to control critical reference voltages, discriminator thresholds and the amplitude of a calibration signal which can be injected by an internal pulser at the input

of the analog channels. Outputs from any or all channels can be killed upon command from a dedicated register.

C. Digital Section

A general description of the digital section and of the output data format is given in [1] for the FSSR prototype chip and will not be repeated here. In FSSR2, a few changes were made. Several DACs were added in the Programming Interface to provide various control functions, as discussed in Section II-B. The 24 bit output data word includes the 3 bits for the ADC pulse amplitude information. The other bits are used as follows: 8 bits for the BCO (Beam Crossing Oscillator) number associated with the hit, 5 bits for the number of the logic set handling the hit, 4 bits for the number of the hit silicon strip, and 1 bit for a word mark (3 bits are unused).

III. Chip Performance

The FSSR2 chip has been successfully tested. Both the analog and digital sections have functioned properly, allowing extensive testing of the chip to be completed. In nominal operating conditions, for FSSR2 the power dissipation (including analog and digital sections) is about 4 mW/channel. The measurement of the critical parameters such as threshold dispersion and ENC was performed by detecting the firing efficiency of the Hit/NoHit discriminator with the threshold scan technique. The experimental results reported here are relevant to measurements performed at room temperature.

A. Charge Sensitivity and Threshold Dispersion

As previously discussed the analog channel can operate in four different peaking time settings, selected by changing capacitor values in the shaper, and in two different gain settings, which are selected by acting on the preamplifier feedback capacitance. Fig. 6 shows measured waveforms at the shaper output at the four t_P settings, in the low gain condition.

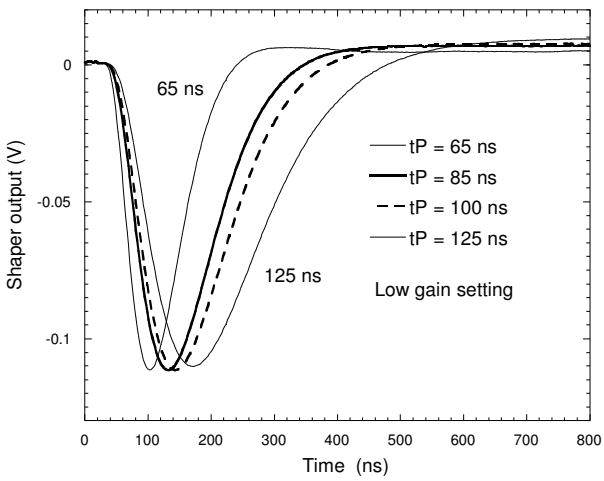

Fig. 6. Averaged waveforms at the shaper output of FSSR2 at different peaking time settings for 1 fC input charge.

The charge sensitivity G_Q at the shaper output is about 120 mV/fC in this condition and is increased up to about 160 mV/fC in the high gain setting, as shown by Fig. 7. This plot compares the measured waveforms at the shaper and BLR outputs, showing the cancellation of the signal tail performed by the BLR. When the BLR is included, G_Q is reduced by about 20%.

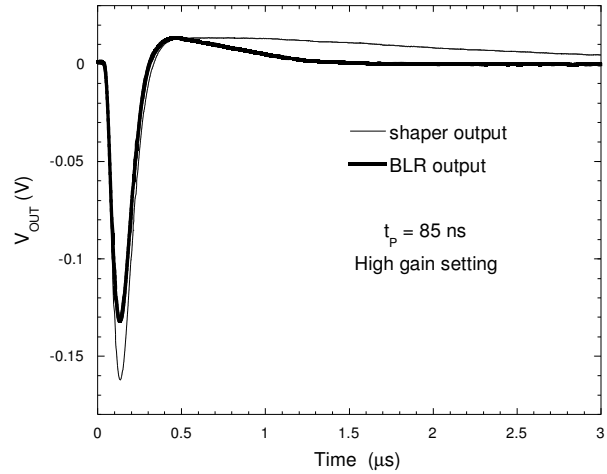

Fig. 7. Averaged waveforms at the output of the shaper and of the BLR at t_P = 85 ns for 1 fC input charge.

Table I shows the measured values of the discriminator threshold dispersion σ_{Qth} expressed in terms of an input charge by dividing the comparator threshold voltage dispersion by the channel charge sensitivity G_Q.

TABLE I
TYPICAL THRESHOLD DISPERSION FOR CHANNELS WITH AND WITHOUT A BASE LINE RESTORER CIRCUIT MEASURED AT DIFFERENT GAIN AND PEAKING TIME SETTINGS

	Peaking time [ns]	Threshold dispersion [e rms]	
		Low Gain	High Gain
Channels with BLR deselected	65	580 ± 50	460 ± 50
	85	600 ± 50	470 ± 50
	125	615 ± 50	485 ± 50
Channels with BLR selected	65	440 ± 40	295 ± 30
	85	440 ± 40	290 ± 30
	125	490 ± 40	280 ± 30

Since the main sources of threshold dispersion are device mismatches in source-coupled pairs in the shaper, BLR and

discriminator, an increase of the charge sensitivity brings along a reduction of σ_{Qth}. The results displayed in Table I show that the presence of the BLR reduces the threshold dispersion. Since the BLR is ac coupled to the shaper output, contributions to threshold dispersion coming from the previous blocks are suppressed when the BLR is selected. As also discussed in [1], the BLR used in FSSR and FSSR2 is effective in removing the threshold shift due to baseline fluctuations of the signal at the shaper output.

Table I shows that the specification σ_{Qth} < 500 e rms is always met in the high gain condition, whereas, at low gain, the BLR has to be selected. Table I and II give also the statistical dispersion of parameter values, evaluated in a set of 10 chips.

Fig. 8 shows the typical response of the ADC to different signal charges. The ADC range was centered around 1 MIP.

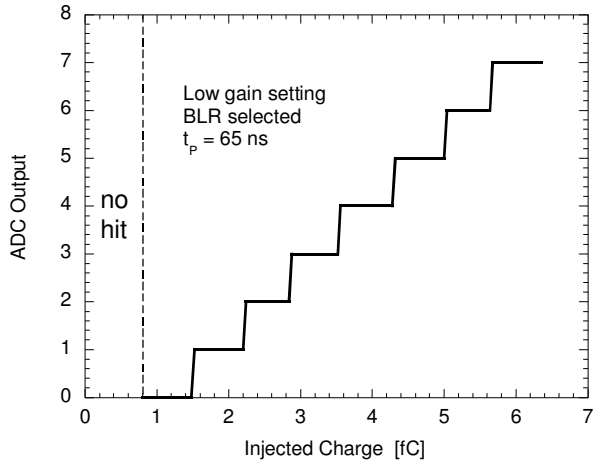

Fig. 8. Measured ADC response in FSSR2. The Hit/NoHit threshold was set at 0.8 fC. The ADC output is expressed in decimal format.

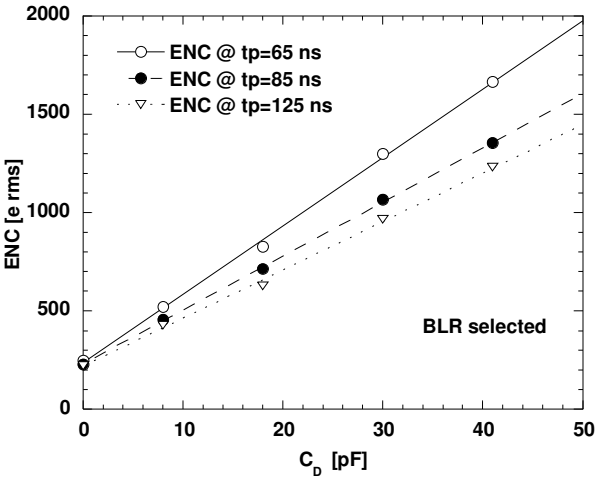

Fig. 9. Measured equivalent noise charge for a channel with baseline restorer selected at three peaking time settings as a function of the detector capacitance C_D.

B. Noise

The Equivalent Noise Charge was measured by fitting the Hit/NoHit discriminator threshold scan data to a complementary error function. Figs. 9 and 10 show the typical ENC values measured for the FSSR2 chip at different peaking time settings. Comparing the two plots, it can be noticed that ENC increases by about 15 % when the BLR is selected. This is in agreement with the expected behavior of a symmetric BLR as that used in FSSR2 [11]. However, the specification ENC < 1000 e rms at C_D = 20 pF is met with a good margin, except at t_P = 65 ns with BLR selected, where ENC is just below 1000 e rms.

Table II reports the values of the ENC sensitivity to the detector capacitance $dENC/dC_D$ at different peaking time settings. Very little variations in ENC are observed if the gain setting is changed.

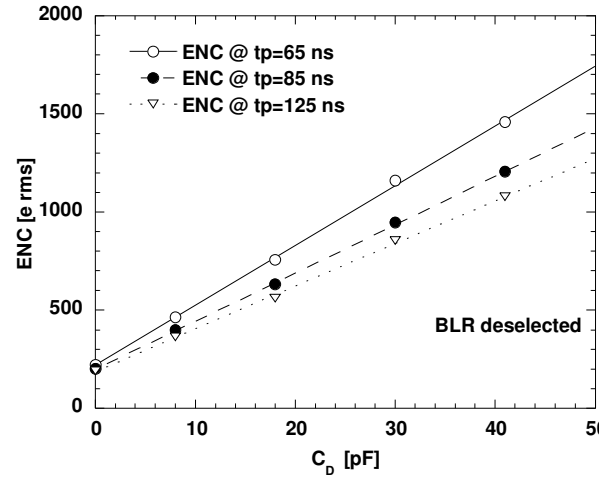

Fig. 10. Measured equivalent noise charge for a channel with baseline restorer deselected at three peaking time settings as a function of the detector capacitance C_D.

TABLE II
TYPICAL EQUIVALENT NOISE CHARGE FOR CHANNELS WITH AND WITHOUT A BASE LINE RESTORER CIRCUIT MEASURED AT DIFFERENT PEAKING TIME SETTINGS

Channels with BLR selected			
Peaking time [ns]	65	85	125
ENC at C_D = 0 [e rms]	240 ± 10	230 ± 10	220 ± 10
$dENC/dC_D$ [e/pF]	35 ± 1	28 ± 1	24 ± 1
Channels with BLR deselected			
Peaking time [ns]	65	85	125
ENC at C_D = 0 [e rms]	220 ± 10	200 ± 10	190 ± 10
$dENC/dC_D$ [e/pF]	31 ± 1	25 ± 1	21.5 ± 1

C. Radiation Tolerance

Different radiation hardness tests were performed on the FSSR prototype and on the FSSR2 chip. Since the chips are fabricated in the same technology and are based on very similar schematics, both using enclosed NMOSFETs, it can be reasonably assumed that the results of FSSR irradiation tests give valuable information about the behavior of FSSR2. In fact, as discussed in Section II-C, the main differences in the analog section between the two chips are the following: a) in FSSR2 the 128 channels have the same input device (NMOS with W/L = 1500/0.45), while in FSSR NMOS and PMOS with different gate length and width are used at the preamplifier inputs; b) in FSSR2 the charge sensitivity is larger than in FSSR; c) critical reference voltages controlling signal shaping and discriminator thresholds are set by internal DACs in FSSR2, while in FSSR they are externally adjusted.

At the SIRAD facility located at the INFN Legnaro National Laboratory [12], the FSSR prototype was exposed to a 1.9×10^{13} cm^{-2} fluence of 27 MeV protons, corresponding to a total ionizing dose of 5 Mrad, that is, the worst case expected for a 10 year operation in BTeV. The proton flux was about 5.5×10^{9} $cm^{-2}s^{-1}$. The chips were irradiated with no bias applied. After irradiation the chip remains fully functional with very little (< 10 %) degradation of critical parameters such as ENC and threshold dispersion [13]. Fig. 11 compares the signal at the shaper output of a channel from a nonirradiated chip and a channel from an irradiated FSSR. Only a slight difference is detected and it is hard to tell whether it should be ascribed to radiation effects or to chip-to-chip variations.

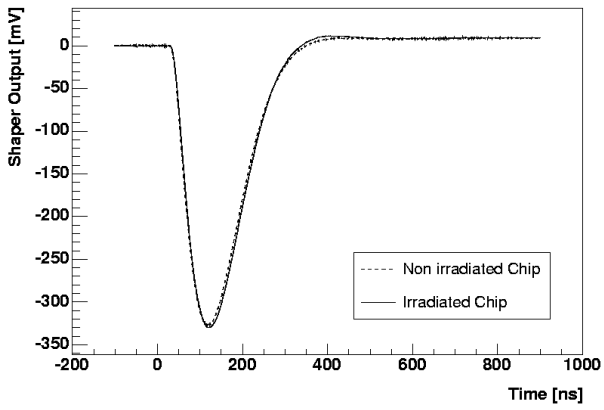

Fig. 11. Averaged waveforms at the shaper output of channels in a non-irradiated FSSR chip and in an FSSR chip exposed to 27 MeV protons at a 4 fC input charge and peaking time setting t_P = 85 ns.

Some samples of the FSSR2 chip were exposed to γ-rays from a ^{60}Co source with a dose rate of about 16 rad(SiO_2)/s. No bias was applied during irradiation. The circuits were exposed to a total ionizing dose of 19.4 Mrad, which is compatible with the radiation environment of LHC experiments. Measurements performed after irradiation show that γ-rays do not seem to affect noise and charge sensitivity. The variation of these parameters before and after irradiation are inside experimental errors and chip-to-chip variations (< 5 %). A larger effect is instead detected in the threshold dispersion when the BLR is selected, as shown by Table III. σ_{Qth} increases by about 15 %, but remains well below the required value of 500 e rms. The increase is smaller if the BLR is not used.

As a general remark, these irradiation tests confirm the high degree of ionizing radiation tolerance that can be achieved in the 0.25 μm CMOS generation.

TABLE III
TYPICAL THRESHOLD DISPERSION MEASURED BEFORE AND AFTER EXPOSURE TO 19.4 MRAD TOTAL DOSE OF γ-RAYS IN THE HIGH GAIN SETTING

	Peaking time [ns]	Threshold dispersion [e rms]	
		Non irradiated chip	Irradiated chip
BLR selected	65	295 ± 30	335 ± 25
	85	290 ± 30	330 ± 25
	125	280 ± 30	320 ± 25
BLR deselected	125	485 ± 50	495 ± 50

IV. CONCLUSION

The 128-channel chip FSSR2 was designed and successfully tested. The device is fully functional and meets demanding specifications in terms of noise and threshold dispersion. Because of its low noise, radiation tolerance and high data output bandwidth and of the flexibility provided by the various programmable features, FSSR2 can operate in different experimental environments and applications. Presently, FSSR2 is being evaluated in view of its possible operation in detector readout in a tracking system providing information to a first level trigger for both fixed target and collider experiments.

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