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THE HERA-B ECAL ELECTRONICS AND MONITORING

The HERA-B ECAL collaboration *

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Table 1: *Parameters of the HERA-B Calorimeter*

	InnerMost	Inner	Middle	Outer
No of channels	400	1700	2128	1728
PM type	R-5600	FEU-68	FEU-84-3	FEU-84-3
LED type	Blue Marl	L934SRCB	L934SRCB	L934SRCB

ABSTRACT

The electronics of the HERA-*B* ECAL is briefly described. The first results of readout chain performance measurements are presented.

1 Introduction

The HERA-*B* Electromagnetic Calorimeter has been designed as a rectangular matrix of 56 by 42 modules made with 'shashlik' technology. It is subdivided into three parts with different granularities: Inner, Middle and Outer sections with 25, 4 and 1 towers per module respectively, being the module a square of about 11 cm side. Each tower is readout with individual photomultiplier(PM). The detailed description of the HERA-*B* ECAL could be found elsewhere [1, 2]. Some parameters of the calorimeter are presented in Table 1.

The ECAL electronics could be subdivided on 4 major parts: Low/High voltage control/supply; Readout; Pretrigger and LED monitoring system.

2 High Voltage Supply

The main goal of the High Voltage(HV) Supply system is to provide the stability of a PM dynode system operation at high particle rates at the HERA-*B* conditions [3] and precise adjustment of the individual channel HV's for gain equalization. The standard solution based on the passive voltage divider with additional HV supply for the last dynodes leads to the high power dissipation per channel and requires a cooling system hardly to realize due to the Inner section fine granularity. An alternative way was chosen to use the Cockroft-Walton(CW) voltage multiplier [4] with a power dissipation smaller than an order of magnitude. Each CW base(see fig.1) contains the clock generator,

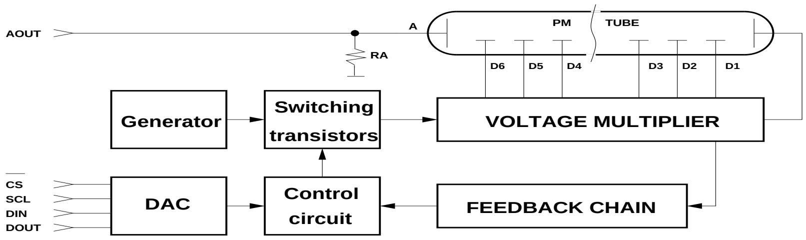

Figure 1: *DC-DC converter base block diagram.*

switching transistors for pumping the diode-capacitor voltage multiplier, feedback chain and control scheme which traces the stability of voltage supplied to the photomultiplier. The last one could be set up by means of 10-bit DAC MAX515 with a precision of about 1 V. Due to relatively small radiation hardness DAC chips are installed outside ECAL for Inner Section, while Middle/Outer bases are equipped with DAC chips directly.

3 LV/HV Control

The main task of the voltage control electronics is to distribute voltages to individual CW bases with the possibility to regulate the high voltage supplied to the individual PM. Overall system is subdivided on six identical parts, each corresponds to left or right half of each section. Each part(see fig.2) consists of VME control board located in the electronic hut and crate EURONORM 9U placed in the experimental area near calorimeter with dedicated controller, high voltage distribution boards and chip select distribution board(for Middle/Outer sections only). Any CW base in Middle/Outer sections is connected with one vertically aligned control(to provide base with clock and data signals and power) and one horizontally aligned chip select cables(to choose vertical coordinate). The matrix like structure allows to address individual channels by standard three wire protocol. Each HV distribution board controls the 8 vertically aligned groups of CW bases. The Chip Select distribution board is used to set up a Y-coordinate on the 1/6 part of the calorimeter. In the Inner ECAL section 25 CW bases corresponding to one module are grouped together on intermediate small distribution board(IM board) on ECAL surface. Each

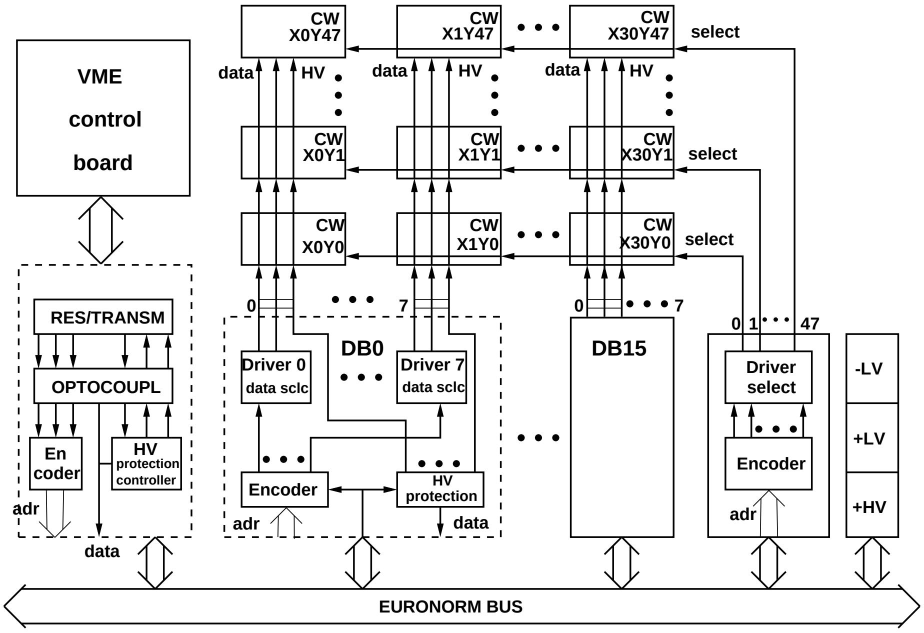

Figure 2: *1/6 ECAL LV/HV Control system.*

IM board is connected with dedicated multi-pin power control cable to the HV distributor. Each Inner HV-distributor controls 4 25-channel ECAL modules also with individual addressing. In addition any HV distributor includes the HV-overcurrent protection scheme. This scheme is allowed to be read out and reset(in case of protection drop).Each crate controller delivers control signals issued by VME control board(see fig.3) over HV distributors.

The protocol implemented is the following(Fig. 4)):

- A RESET signal(100 ns) is send by VME to the Crate Controller. As a consequence the CTRL register of the controller is set to 0, controller preset counter is set to 31, two VME board registers READY_TO_LOAD and DATA_SENT are set to 0.

- The DATA and XY_SELECT patterns are written on two VME board registers(32 and 16 bits respectively). In the DATA pattern 10 bits are

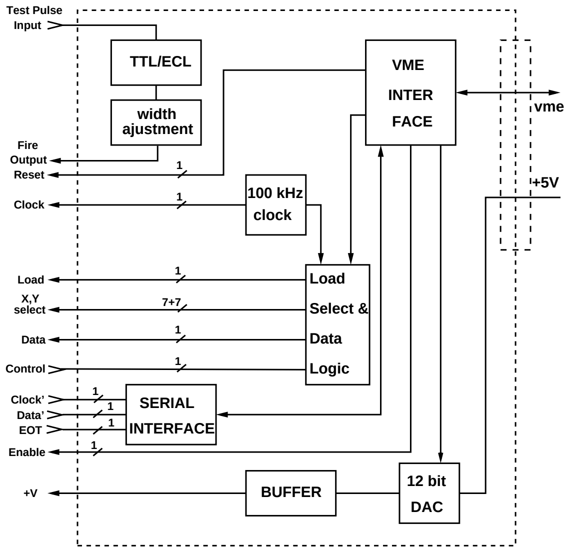

Figure 3: *The ECAL LED/CW VME configuration board block diagram.*

reserved to setup high voltage value. Others are defined by internal peculiarities of DAC chip configuration protocol. Bits 0-6 of XY_SELECT pattern contain X-address, bits 8-14 - the Y address. Bits 7 and 15 are not used. 3 bits of X-address are defining the number of vertical group of CW bases(Middle and Outer) or column on IM board(Inner) and 4 other bits - number of distribution board in crate. For Middle/Outer type distribution board 6 bits of Y-address are to choose the chip-select line(0-47). In Inner type board Y-address 3 bits are defining a line on IM board and 2 bits are defining number of one IM board out of 4.

If the Y-address 7th bit is set up the DATA pattern will be written to the CW base, otherwise HV protection will be reset.

- The internal register READY_TO_LOAD is set to 1 and then a LOAD pulse(100 ns) is sent to the controller.
- After about 1 μs a train of 32 clock cycles at 100 kHz frequency together with the DATA serial pattern is sent to the controller.
- As soon as the transmission is ended the controller preset counter should be zero and CTRL level should be transmitted by the controller to the

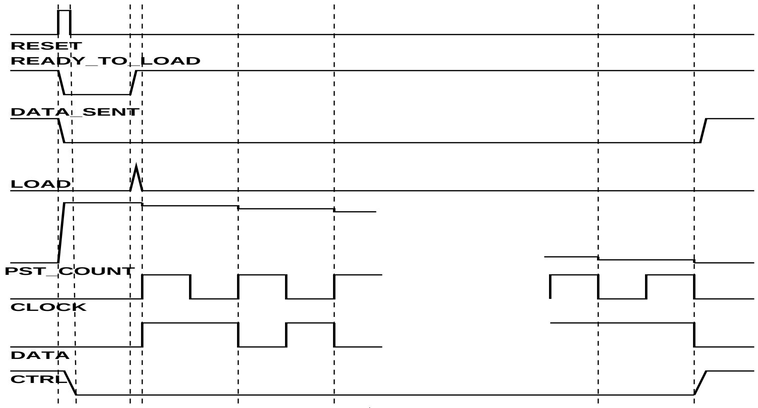

Figure 4: *The logic of LED/CW system configuration.*

VME board. This level is written in the DATA_SENT register.

- The DATA_SENT register is read in a pulling mode. When it is 1 a new cycle can be started. If it is not 1 after a timeout an error message is issued.

In addition the Crate Controller could send a serial DATA' 256 bits pattern via a 100 kHz CLOCK'. This pattern contains the status of the HV protection for all channels from 1/6 part of ECAL. The protocol is the following:

- when a VME board is ready to receive data from the controller, the board ENABLE register is set to 1 and a DATA_READY register is set to 0.
- A DATA' serial pattern of 256 bits is send by the controller together with 100 kHz CLOCK'. The last 8 bits of this pattern store control sum. The serial pattern is converted to parallel in blocks of 32 bits and stored into 8 32 bit registers.
- At the end of the DATA' transmission a EOT signal of 100 ns duration is sent by Controller. The DATA_READY register as a consequence becomes 1 and the ENABLE level is 0.

The VME control electronics in the electronics hut is optocoupled from controllers to avoid grounding loops.

4 Readout and pretrigger

The main goals of ECAL readout system are to:

- provide fast digitization of the PM analog signals(Implemented by means of a 10 MHz 12-bit flash ADC)
- store the events during the time the First Level Trigger(FLT) system generates a decision. The events selected by the FLT are transmitted to the HERA-B DAQ system. This storing pipeline is realized by means of Dual Port Ram (DPRAM) organized as a circular buffer of 256 events deep.
- prepare 8 bit digital compressed word from pedestal subtracted and converted to absolute energy units ADC data and feed this word synchronously to the ECAL pretrigger system. This conversion is achieved by means of programmable LookUp Tables.

The ECAL pretrigger is an asynchronous system that provides electron/positron candidates to the FLT with latency of about 3 μs. It allows to measure energy of clusters, to perform the calculation of the shower center of gravity and to recover electron/positron energy loss via bremsstrahlung(the last one improves the resolution on the J/Psi reconstruction at the FLT level). Design of ECAL Readout/Pretrigger systems is already described(see for example [5]) and we will not concentrate on it in this paper.

5 LED monitoring system

The LED monitoring system is designed to provide the control of the readout chain behaviour,a monitoring of ECAL channels stability and physical signals emulation for pretrigger test purposes. Each PM-channel is equipped with individual LED(blue ones for the InnerMost section and red ones for the rest of ECAL). The LED pulse amplitude is adjustable and covers all the ADC dynamic range.

The monitoring chain(fig.5) consists of LED drivers and LED distribution boards placed on the detector surface and of VME control board in electronic hut. The LED drivers and the LED distribution boards are connected with matrix-like set of horizontally/vertically aligned flat control cables. One such a chain attends to 1/16 of whole ECAL. LED drivers(see fig.6) are placed in the front of each calorimeter module and they consists of LEDs(1 LED per each ECAL tower), shift register, LED driver and fire signal width control

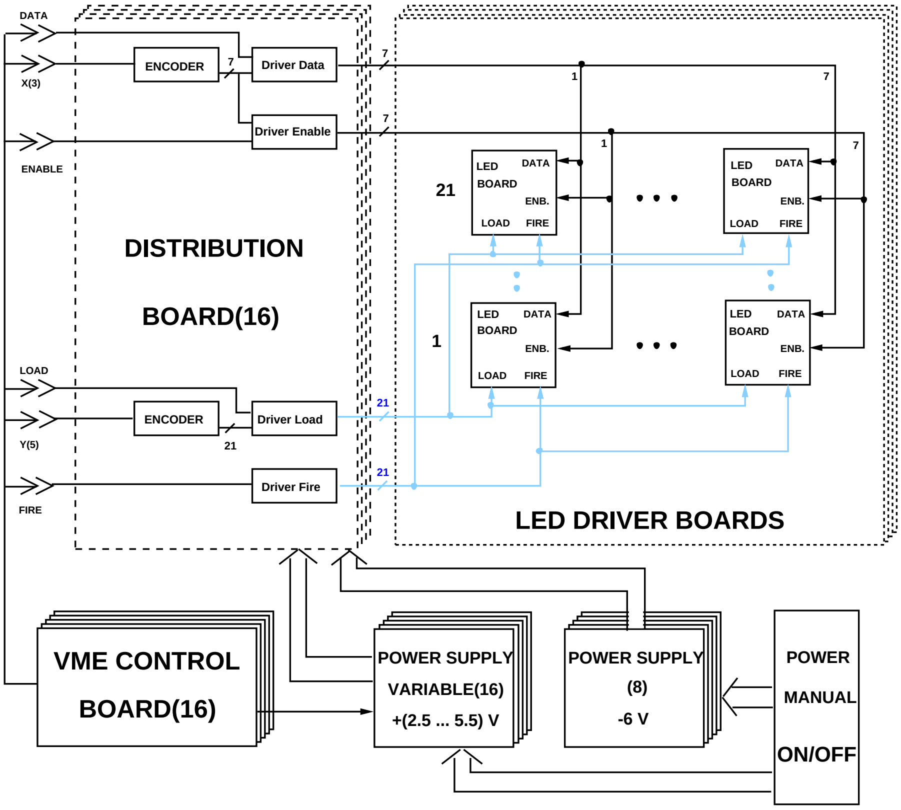

Figure 5: *LED system general view.*

scheme(for INNER section only). The last one allows to vary the duration of LED fire signal from 5 up to 12 ns with step 1 ns.

VME control board(fig.3) issues control signals(read/write, data, address and so on) and analog voltage to vary light pulse amplitude. The LED distribution board forms and delivers LED fire signals over corresponding LED driver boards as well as feeding them with low voltages and allowing to set any desirable pattern. The protocol implied is the same as for the CW system, described above, except:

- The DATA pattern contains 32 bits and defines the LED map to be fired in ECAL module(1, 4 and 25 bits for Outer, Middle and Inner sections

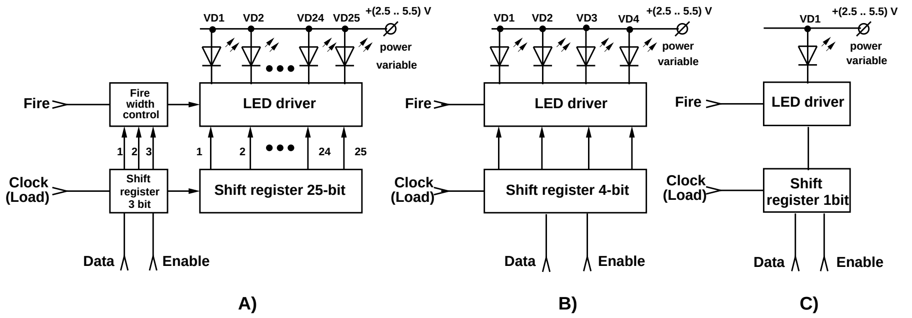

Figure 6: *Circuit of the LED driver board: A)Inner B)Middle C)Outer sections.*

correspondingly). For Inner section the 3 most significant bits define the value of the fire pulse width.

- The X/Y-addresses defines the number of horizontal/vertical control cables to select ECAL module.
- A 12-bit VME programmable DAC allows to adjust the LED voltage from 2.5 to 5.5V.
- VME control board interacts directly with the dedicated LED distribution board.

Normally LEDs are fired with frequency about 10 Hz in coincidence with one of the "empty" HERA bunches(prescaled HERA cycle). That allows to trace individual channel stability directly during data taking.

6 Readout chain performance

The stability of the overall readout chain was traced for Inner/Middle sections using different methods during time period more than 1.5 months before HERA shutdown: control of overall π^0 and η peak position in different sections(using only pure ECAL information), individual LED position fluctuations(readout and LED systems instability), E/P peak position(ECAL and tracker system instability). The results are reported in Table 2) and seems to be compatible

Table 2: *Results of the Readout chain stability measurements on 45 days*

	π^0 and η	LED	E/P	Pedestal
Mean pos. variation	2%	2-3%	3%	1.25 ADC ch.

among themselves with a stability of the ECAL readout chain on level of 2%. It should be emphasized that with the methods applied it is hard to achieve a better accuracy for stability estimations and the numbers presented could be considered as an upper limits.

The pedestal position was stable on 1.25 ADC counts level, that is compatible with the pedestal determination accuracy. The number of hot channels(due to damaged CW bases and ADC) in calorimeter Inner/Middle sections is less then 0.2 percents and the number of dead channels in these sections does not exceed 3.5% level.

7 Conclusions

During last 2 years of data taking control, readout and pretrigger electronic was installed and fully commissioned. Overall readout chain shows a good performance: stability better than 2% and acceptable numbers of hot/dead channels. For all the known problems solutions are already found and will be implemented during the HERA shutdown in the period 2000/2001.

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