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Proposal for a Level 0 calorimeter trigger system for LHCb

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Abstract

In this note we present a complete system for the Level-0 LHCb calorimeter triggers. The system is derived from the electromagnetic calorimeter pre-trigger developed for the HERA-*B* experiment. The proposed system follows closely the Level-0 trigger algorithms presented in the LHCb Technical Proposal based on an electromagnetic and hadronic showers analysis performed on 3x3 calorimeter matrix. The general architecture presented is completely synchronous and quite flexible to allow adaptation to further improvements on the Level-0 trigger algorithms.

1 Introduction

This note develops and updates the basic ideas of our proposal for a Level 0 (L0) calorimetric trigger for the LHCb experiment presented for the first time in the previous note [1]. These ideas have been developed starting from

our experience in the HERA-B experiment where we proposed and built an analogous project (see Ref. [3]).
As a preliminary remark, one would note that the requests for the LHCb experiment L0 calorimeter trigger are less demanding with respect to the HERA-B electron pre-trigger system. The main point in this respect, is that due to the necessity of exploiting the full power of the machine to collect sufficient statistics, we designed an asynchronous logic for the HERA-B pre-trigger which fulfills also the task of recovering the energy lost by electrons via brehmsstrahlung. In LHCb, conversely, the physics requirements can be satisfied in the frame of a **synchronous logic** which simplify considerably the architecture and the design of the board originally proposed for HERA-B, getting significant gain, at the same time, in system **robustness** and **debugging capability**. In spite of the numerous possible simplifications, we are convinced that it is of relevant importance to adopt technical solutions which preserve the generality of the system (like the **flexibility in the L0 algorithm** that can be implemented and the capability to **produce more than one candidate** per event analyzed). This, taking into account the wide physics program of LHCb, could represent a decisive advantage in future investigations on reaction channels up to now not considered.
The present note is composed by several sections. After the presentation of the assumed framework and the general overview of the project (Section 2), we discuss the electronic block scheme for the ECAL L0 trigger (Section 3), for the HCAL L0 trigger (Section 4), the plan of the connections (Section 6), the problem of debugging and monitoring (Section 5) and the evaluation of the cost (Section 7) of the proposed trigger board. The simulations and the detailed evaluation of the performances are actually in progress; nevertheless significant and useful information can be extracted from the experimental data collected during the development of our HERA-B project (Section A).

2 General aspects of the project

As shown in Ref. [4] in the case of LHCb photons represent the main fraction of events having large p_T. For this reason, to design efficient electron and hadron triggers, it is necessary to reject the large photon component and to complete the system of electromagnetic and hadronic calorimeters (ECAL and HCAL respectively) with preshower (PS, electron/hadron separation) and PAD (neutral/charged separation) detectors. According to these considerations, the boards of electron and hadron triggers must handle, in addition to the ECAL and ,eventually, HCAL signals, also PS and PAD signals. The details of the logic will be explained in the following.
The overall geometry of the involved detectors is assumed from Ref. [4] and almost coincides with the one foreseen in the letter of intent (LOI). Concerning

the details of the segmentation we adopt the one described in Ref. [5] which foresees cell sizes of 4 and 12 cm in ECAL and 12 and 24 cm in HCAL. The segmentation of PS matches exactly the one of ECAL, while a $2:1$ correspondence in X (bending plane) and $1:1$ correspondence in Y is assumed for the PAD system as described in Ref. [4]. The relevant feature of the segmentation of the involved detectors is the projectivity, which allows to establish an easy correspondence between the respective signals, since the details are not important and do not affect the architecture of the proposed trigger card. The double segmentation proposed in Ref. [5], even if it does not allow a relevant saving in the number of channels with respect to the more performant triple segmentation assumed in the LOI (Ref. [4]), could be justified from the point of view of an easier mechanical assembling of HCAL modules. The detailed segmentation, however, is not definitive and, if necessary, could be modified.
We plan to connect each 4x8 matrix (4 along X and 8 along Y) of calorimetric cells to a 32 channels front-end (*fed*) card. The signals of each *fed* card can be transmitted to a dedicated L0 trigger card by means of a driver based on cheap LVDS transmitter (see Section B). Each L0 card processes, independently from the others, the signals of one *fed* card in order to select the highest p_T shower. Following Ref. [4] we propose to use an algorithm based on

i) search of the 3x3 cell with highest energy [1] deposition;
ii) evaluation of the impact point by means of the center of gravity (COG) of the energy depositions in a region of 3x3 cells centered at the cell candidate of highest energy.

To perform the calculation of the COG with no losses due to boundaries among L0 cards, we foresee to transmit, in addition to the content of the 32 channels of the ECAL *fed* card, also the signals of the 28 neighboring cells. Note that in the proposed implementation the problem of **ghosts** (energetic clusters developing between two L0 cards) is absent; this means that, if further developments of the L0 algorithm will require it, it will be possible to send to the L0 Decision Unit (L0DU) not only the highest transverse momentum cluster but also other clusters without the problem of ghosts cleaning .
The proposed algorithm can be translated into a logic which is **completely synchronous**. One of the limit imposed by a synchronous logic consists in the necessity of treating only one candidate in each L0 card. This seems not to be a severe limitation due to the fact that each L0 card processes the signals of a matrix of calorimetric cells which has a small spatial extension.

[1] The ECAL (and HCAL) *fed* cards performs a conversion on readout data by means of look-up tables by coding the 12 bit ADC response in 7 bit.The general structure of the proposed system does not change if the result of the coding is an energy or a transverse momentum.

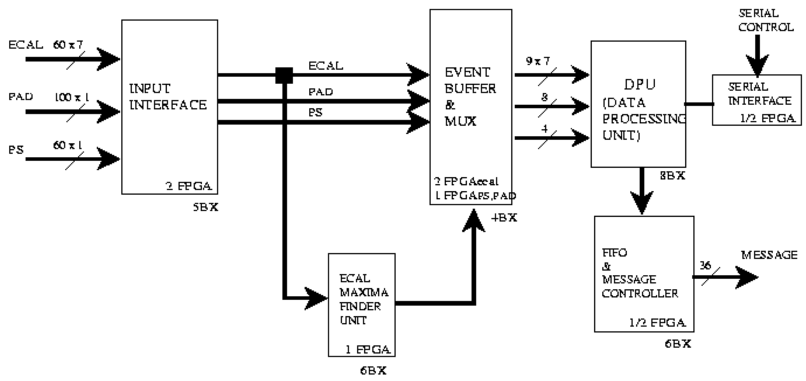

Fig. 1. Block scheme of the proposed design for the L0 ECAL card.

3 Outline of the L0 ECAL system

In this section we will describe the logic blocks for the L0 ECAL system (see Fig. 1). The algorithm implemented with this logic is essentially the one presented in Ref. [4] and derived from the LHCb TP(see Ref. [2]). The only simplification is that the present algorithm makes a selection of the center of the 3x3 matrix based on the maximum transverse energy release in a single cell of the 8x4 matrix handled by a L0 ECAL card. We think that this is a quite reasonable assumption due to fact that the expected occupancy per calorimeter cell for minimum bias events in ECAL is 5-10% (with an energy threshold of few hundreds of MeV). The inclusion of the HCAL system will be described in Section 4.
The system consists of 9U VME cards handling 32 (a matrix of 8x4) ECAL *main* towers each.
A schematic overview of the overall proposed system for the L0 ECAL trigger is shown in Fig. 2. A *main* tower is the central one in a basic 3x3 matrix. In order to form all the possible 3x3 matrix relative to the 32 *main* towers handled by a card we need also that 28 *border* cell signals are available in the card itself.
Starting from this considerations a 9U VME card will accept as input:

- 32 *main* and 28 *border* ECAL single tower signals;
- 32 *main* and 28 *border* Preshower (PS)signals;
- 64 *main* and 36 *border* Pad Chamber (PAD) signals.

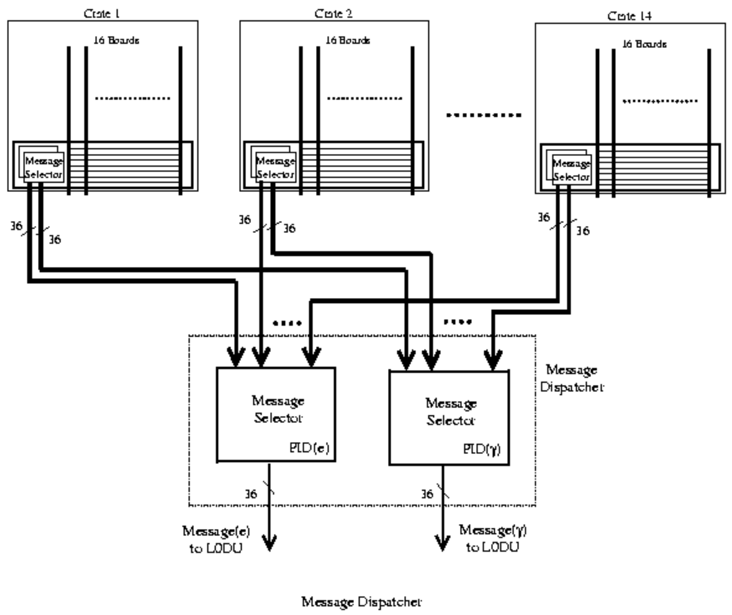

Fig. 2. Overview of the overall L0 ECAL system.

The ECAL single tower energy signals are energy (or p_T) coded on 7 bits, while the PS and PAD signals are coded on 1 bit.
The *main* signals are received directly from the ECAL, PS and PAD *fed* cards respectively, while *border* signals are exchanged by means of the L0 cards themselves via backplane or via short connections on copper.
The Input Interface (IIF) block receives all these signals from the various detectors *feds* and from the neighbor L0 cards and foresee proper delay in order to time-align the events. The data transmission from the various detectors *feds* is, up to this point, synchronous. The following event processing in the L0 card is synchronous too, **so that no signal pipelining and storing with a bunch crossing (BX) addressing is needed for the IIF**.
The ECAL energy signals (60x7 bits) are sent to a Maxima Finder Unit (MFU) that extracts, in a pipelined mode, the maximum deposited energy within the 32 *main* ECAL tower signals after inspection also on the *border* signals.
The address of the cell having the maximum deposit of energy (central tower in a 3x3 matrix) is passed to the Event Buffer and Multiplexer (EB). The EB extracts , from the IIF and in a pipelined mode, all the relevant information needed for the L0 ECAL trigger algorithm, i.e.:

- the nine 7 bit energy values of the 3x3 matrix centered on the ECAL candidate;

– the 4 bit [2] of the PS needed (see Ref. [4]) for hadron/em identification (ID);
– the 8 bit of the PAD needed (see Ref. [4]) for charge/neutral ID.

All this information is sent to the Data Processing Unit (DPU) (entirely designed with lookup tables (LUT)) which working in pipelined mode, extracts:

– the total ECAL cluster transverse momentum after applying a threshold cut;
– the center of gravity of the ECAL cluster;
– a particle ID (PID) signature on the nature of the ECAL cluster (electron/photon/hadron).

The LUT's design of this unit **adds flexibility** to the possible L0 algorithms which can be implemented, as it will be shown this in Section 3.4.
If a valid candidate has been detected the output messages from DPU contain the following information:

– Total ECAL cluster transverse momentum: 7 bit;
– ECAL cluster horizontal center of gravity coordinate: 10 bit;
– ECAL cluster vertical center of gravity coordinate: 9 bit;
– PID signature: 2 bit;
– BX number: 8 bit.

It has to be noticed that, up to the DPU output, **the designed system is still synchronous**.
The message outputs from the DPU is collected by a Message Selector (MS) logic block built onto the backplane. This logic unit

– performs a selection on the message type based on the PID;
– finds the maximum transverse momentum for each PID for the 16 boards of a VME crate;
– sends, for each crate, the message relative to the maximum transverse momentum for each type of particle (electron or photon) to a completely analogous MS logic block built on VME cards (Message Dispatcher -MD-).

There is one MD card collecting the messages coming from each VME crate.This card performs a further search of the maximum transverse momentum message (separately for electron and photons) among the ones sent by the VME crates and sends it to the L0 decision unit.

[2] Note that the number of bit needed from PAD and PS for signal validation is assumed under the hypothesis of Ref. [4] (non projective geometry). These numbers could be different in the case of projective geometry without affecting the principle of the proposed logic for the L0 card.

Table 1
ECAL L0 trigger logic blocks and their latency in LHCb clock cycles.

LOGIC BLOCK	LATENCY LHCb clock cycles
Input Interface (IIF)	5
Maxima Finder Unit (MFU)	6
Event Buffer and mux. (EB)	4
Data Processing Unit (DPU)	8
Message Selector (MS)	4
Message Dispatcher (MD)	4
TOTAL	31

In Table 1 the expected latency for each logic block is reported.
The L0 ECAL system works entirely in pipelined mode at a 40 MHz clock frequency and is **completely synchronous**.

3.1 Input Interface

The IIF is essentially composed by several data receivers to get the signals coming from the front-end cards in differential format. Under the hypothesis of using the commercially available and cheap DS90CR285 transmitter / DS90CR286 receiver pair, at every cycle of the transmit clock, 28 bits of input data can be transmitted. The DS90CR285 transmitter in the readout board converts 28 bits of CMOS/TTL data into 4 LVDS (Low Voltage Differential Signaling) data streams. Each DS90CR286 receiver in the IIF converts the LVDS data streams back into 28 bits of CMOS/TTL data. This multiplexing of the data lines provides a substantial cable reduction (see Section 6).
These LVDS receivers are able to work at a clock frequency of 66 MHz with a cable up to 10 meters; we have performed a set of preliminary measurements with these devices at 40 MHz (LHC timing) with data transfer on normal twisted pair cables having 10m length (see B).
The IIF can be realized using two FPGAs and the evaluated latency is 5 LHCb clock cycles (to allow for time alignment of signals coming from different detectors).

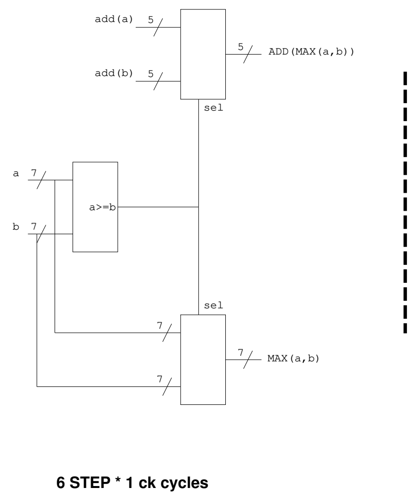

Fig. 3. The fundamental block logic for the MFU.

3.2 Maxima Finder Unit

The Maxima Finder Unit (MFU) is a device that finds the absolute maximum in a 4 x 8 matrix. It can be implemented in one Field Programmable Gate Array (FPGA). At the beginning 16 pairs of cells are compared . At the second level these 16 results are compared with 8 comparator, and so on. In this way we need log2(32)=5 levels to obtain the absolute maximum in the 4x8 matrix. Each level can be implemented in one clock cycle (see Fig. 3) and then the latency can be estimated in 6 BX.

3.3 Event Buffer and Multiplexer

The EB (see Fig. 4) stores the 4x8 matrixes in an event buffer composed by static RAMs implemented in commercial FPGAs. The address of the maximum found by the MFU is sent to the EB; the multiplexer in the EB selects the 3x3 matrix having this maximum as central cell. The data extracted are sent to the LUT by means of 9x7 bit bus. The ECAL part has 60x7 bits in input and 9x7 bits in output. To handle this large number of bits we need two FPGAs to perform the event buffer function for the ECAL signals. Another FPGA must be considered for buffering and multiplexing the PAD and PS signals. The latency of this pipelined block is estimated in 4 BX,since in the HERA-*B* pre-trigger the same function is performed in 4x24 ns.

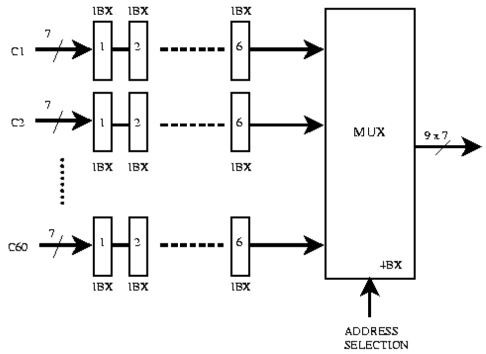

Fig. 4. The interfacing block scheme to the Event Buffer and Multiplexer for the ECAL L0 card.

3.4 Data Processing Unit

As mentioned, the DPU is a very flexible block, entirely designed with LUTs, which allows in principle to perform a large variety of trigger algorithms.
In order to preserve this characteristic and to allow, for instance, further development of the trigger algorithm during the LHCb running, one could think of a modular L0 ECAL trigger board composed by a mother board, containing all but the DPU logic blocks, **and the DPU itself, realized on a piggy-back card mounted on the mother board**.
To give an example of how flexible the trigger algorithm a DPU can be, we will describe the block diagram shown in Fig. 5.
The DPU shown in this example accepts as input the following signals:

- 3x3 matrix of 7 bit energy values centered around the ECAL candidate;
- PAD information for the ECAL candidate on 8 bit (see [4]);
- PS information for the ECAL candidate on 4 bit(see [4]) ;

The algorithm performed by the DPU with these input signals is the following:

- evaluation of the ECAL cluster total transverse momentum on the 3x3 matrix centered on the ECAL tower with maximum deposit of energy;

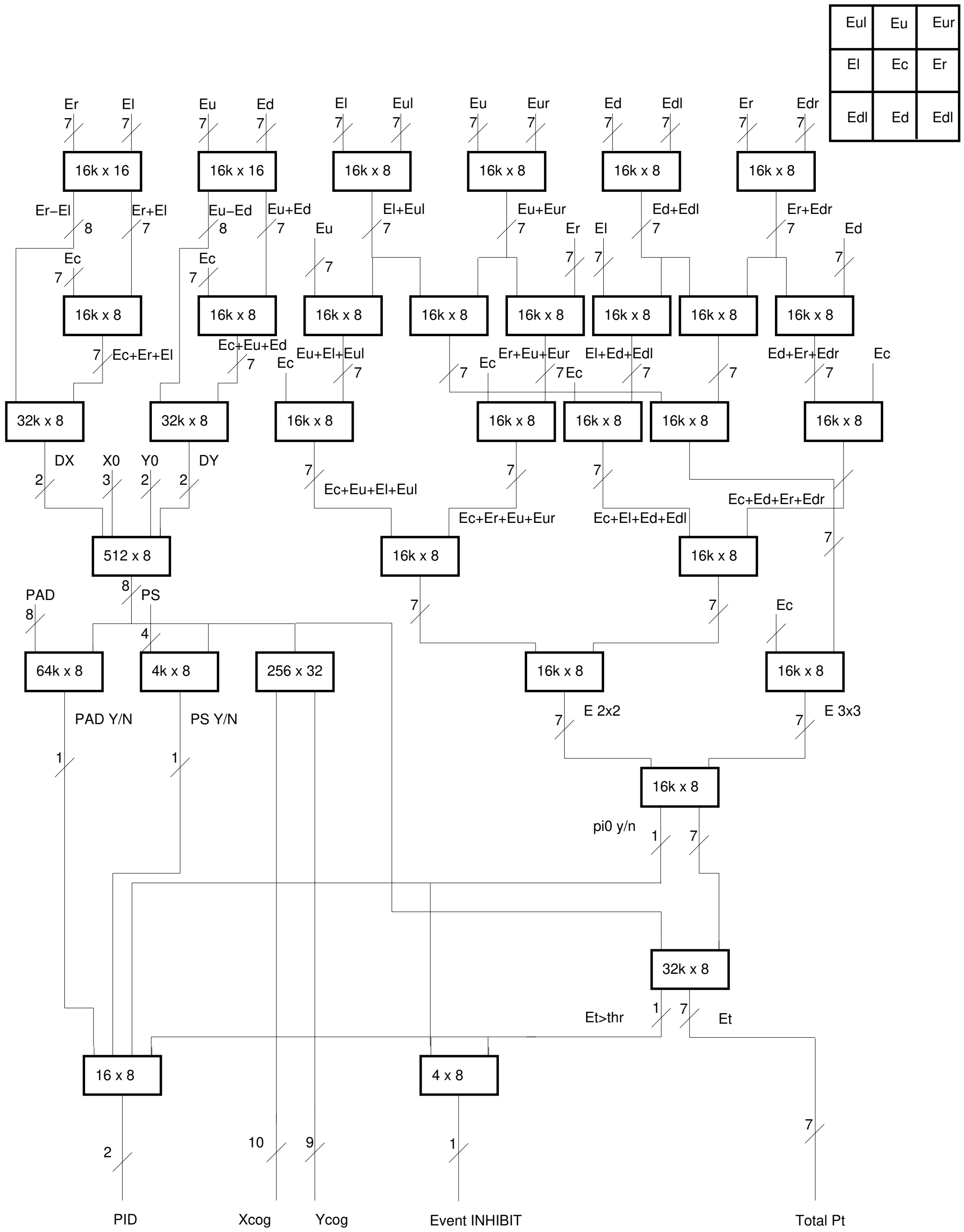

Fig. 5. A possible DPU block diagram for the L0 ECAL trigger board. This block can be adapted to different L0 algorithms, also including, for instance, signal from HCAL.

– evaluation of the ECAL cluster center of gravity on the 3x3 matrix;
– A PID is given based on the information given by ECAL, PAD and PS. The algorithm performed for PID is the one presented in Ref. [4]
  In addition, the DPU performs:
– evaluation of the ECAL cluster total transverse momentum on the 2x2 matrix centered on the ECAL tower with maximum deposit of energy. Of the four possible 2x2 combinations the one with maximum energy is chosen.

– evaluation of the ratio of the energy deposited in the 2x2 and in the 3x3 cluster. If the experimental data will confirm the simulation result that most of the cluster energy is deposited on a 2x2 matrix, this ratio could be used for energetic π^0 signature (most of the photons from the decay of energetic π^0 have small opening angle and tend to deposit their energy, eventually overlapping themselves,in a small ECAL area). This signature could be added in the PID decision LUT or used for π^0 rejection (see Section A.2 in the Appendix). In this last case an improvement in the signal to background ratio could be expected,for instance, for the hard photon triggers.

To summarize, with the DPU structure described, we see how we have the flexibility to choose between an ECAL and HCAL L0 algorithm like the one presented in Ref. [4] or one algorithm derived from a 2x2 clusterization [3] .The total amount of LUT memory for this DPU is about 600 kBytes and the total latency is 8 LHCb clock cycles.

3.5 Message Transmitter and Serial Interface

The MT stores the data coming from the DPU and send it to the MS. The Serial Interface is intended for slow control operation in the board (LUT loading, system debugging etc.). The message transmitter and the serial interface can be realized in the same FPGA.

3.6 Message Selector and Message Dispatcher

In each crate, a MS , built onto the backplane, evaluates the highest value of transverse momentum and sends the message with this p_T value to an analogous MD logic block built on VME cards. The selection (see Fig. 6) is performed in a block composed of log2(16)=4 levels of comparators to obtain the absolute maximum in a crate with 16 boards. Each level is implemented in one clock cycle and then the latency can be estimated in 4 BX .[4] The

[3] It has to be noticed that the 2x2 clusterization algorithm that can be implemented differs from the one presented in Ref. [5] in the selection performed by the MFU.In our proposal the 2x2 matrix is evaluated around the most energetic single cell signal in one board.

[4] The proposed scheme for the MS and MD can be easily adapted for the **search of the second highest p_T cluster**.The highest p_T value is masked and a second search for maximum p_T is performed on the remaining messages both at the MS and MD. This operation adds a 4 clock cycles latency in the MS and in MD. The total expected latency for the L0 ECAL trigger in this case becomes 39 clock cycles (compare with Table 1).

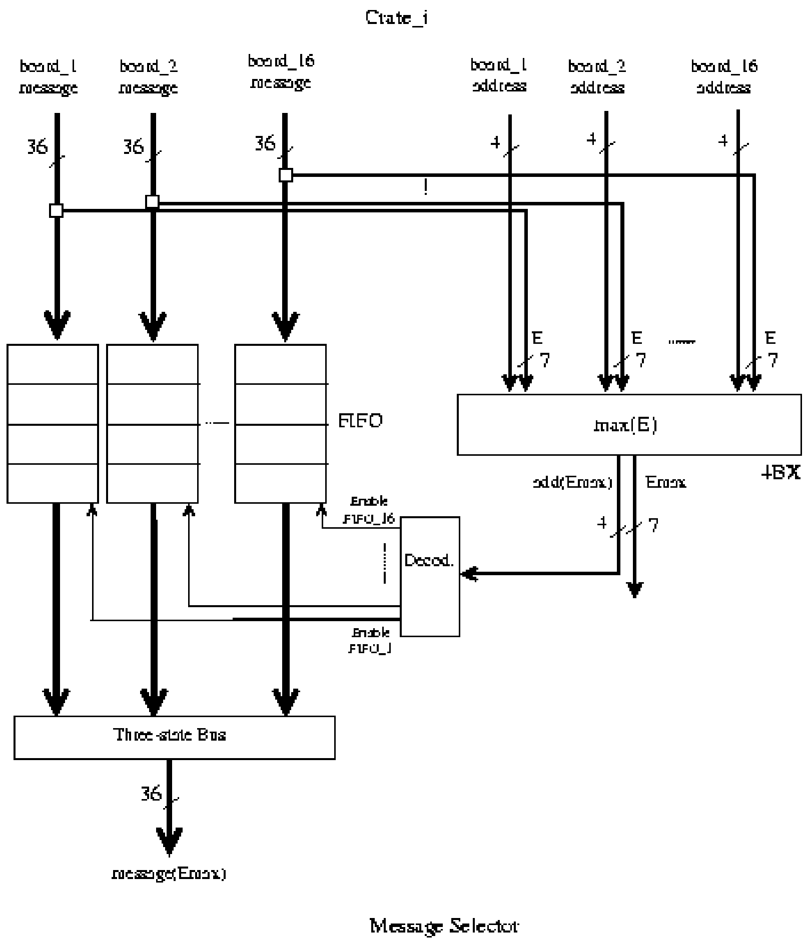

Fig. 6. The Message Selector logic block. This block is built onto the VME crate backplane. An analogous block is built into the Message Dispatcher VME card.

result of this block is used to enable the FIFO where the message has been held during the 4 clock cycles.
The Message Dispatcher is composed by one board that select, depending by the PID (photon or electron), the message with the maximum value of the p_T. The board contains two message selector blocks (one for electrons and one for photons) in which the total latency is again 4 clock cycles . The two messages (one for the electron and one for the photon) with the highest p_T value is sent to the L0DU. With this architecture **all the operations of the L0 ECAL trigger are synchronous**.
Note that a control can be performed both on the MS and MD logic blocks in order to check the consistency of the BX identifier coming from the L0 cards and from the L0 crates. An **error flag can so be added to the output messages to detect the appearence of missing clocks**.

4 The HCAL L0 system

The actual status of definition of the HCAL geometry (mainly in the correspondance between ECAL and HCAL calorimeter towers) and of Monte Carlo simulation is such that at the moment we propose an HCAL L0 trigger scheme not using the ECAL information. To keep ECAL information separated from the HCAL L0 trigger leads to an enormous simplification in trigger logic and connections; these are considered a quite strong motivation not to complicate the L0 trigger implementation and to keep the cost of the realization low.
It has nevertheless to be stressed that this simplification has been evaluated (see Ref. [4]) to lead to a relative 10% reduction in efficiency for the $B_d^0 \to \pi^+\pi^-$ channel while keeping a suppression factor of about 16 in the regime envisaged for the L0 trigger. This reduction in efficiency can not be considered negligible and, if the forthcoming Monte Carlo simulation will confirm it, an effort is needed to optimize the presented implementation.
In order to implement the algorithm described in Ref. [4] it is clear that the solution at hand is to use a simplified version of the logic blocks used in the L0 ECAL card. The simplification is that PAD and PS signals are not needed for the HCAL L0 trigger.
The system is **completely synchronous**, and the capability of the designed system to provide the L0DU also with the **second highest energetic cluster** without heavy conceptual complications in the design (as explained in Section 3.6) has to be considered as an important point for the HCAL trigger purposes.
In the case that in the next future the relevance to add HCAL information with the ECAL ones would be considered important the strategy adopted could be the following:

– Form the highest p_T 3x3 (or 2x2) cluster on the HCAL *fed* cards. Note that in the case of hadron calorimeter the energetic resolution is poorer: no *fed* data compression is needed and to give the center of cluster cell address is probably enough for the L0 purposes. The relevant informations can be obtained by means of logic adders (once the *fed* data are converted in p_T values). The overall latency to get the highest p_T cluster value and address for each card is less that the one needed for the ECAL L0 cards at the DPU output.
– The output messages from each HCAL L0 cards are directed to the proper ECAL L0 MS.The gain in latency, with respect to the ECAL L0 trigger, up to this point, can probably allow a HCAL data reorganization and proper combination with the messages coming out from each ECAL L0 card to form a HCAL L0 trigger that takes into account also the ECAL information on high p_T clusters.

In the two described solutions ("without" and "with" ECAL) the latency scheme presented in Table 1 is unchanged. In the evaluations presented in the following Sections we will refer to the HCAL L0 solution "without" ECAL for the evident reason that the alternative solutions has to be properly developed.

5 System debugging and monitoring

The designed logic for the L0 trigger cards is quite complex and a detailed debugging strategy has to be foreseen to allow for a reliable realization of the system in all its phases. For this reason we intend to implement the "boundary scan" technique described in the following. JTAG (IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture) is a set of standards for board test protocol by means of the boundary scan technique. It is is a 4-wire standard which allows interconnect testing. Adding boundary scan to a board does add cost and time to the design cycle due to the increased cost of boundary scan components and initial time investment required to understand the boundary scan architecture and tools. However, these costs are easily justified when viewing the benefits and cost savings which boundary scan provides at every stage of a board's life cycle. A designer uses boundary scan to save time during the prototyping and design debug stage. With boundary scan, non design-related, structural faults can be detected and then eliminated at both the board level and component level. This allows designers to effectively locate and resolve design related problems. Additionally, designers use boundary scan to partition a board, and/or load internal values into device registers to isolate logic errors. The IEEE 1149.1 standard defines a 4 pin TAP (Test Access Port) which allows electrical access around the"boundary" of devices. The TAP pins are: TDI Test Data In, TDO Test Data Out, TMS Test Mode Select, TCK Test Clock. It also defines a 16 state TAP Controller and several

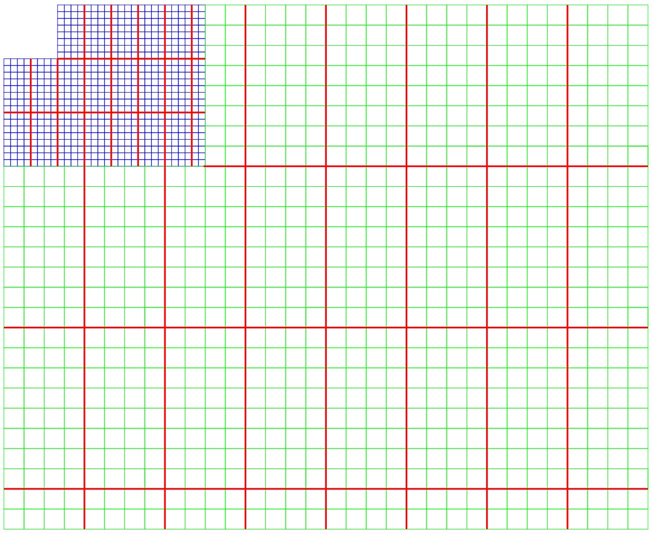

Fig. 7. An ECAL quadrant and its partition in ECAL L0 boards.

registers used to control the test data. Boundary scan registers are placed at all I/O pins, and they are interconnected to form a serial chain around the core functionality of the device. With the addition of the boundary scan registers at the I/O of a component, interconnect testing with boundary scan devices can be performed with no dependence on device functionality.
This kind of testability represent a part of the whole debugging system. Another important part will be the "slow control" system. For this task we will use another serial interface, in addition to the JTAG port, implemented also on a FPGA (see Fig. 1). This serial interface will be used for the following purposes:

– loading and monitoring the L0 card LUT memory;
– loading and monitoring the FPGAs programs;
– test and debugging the L0 card functionalities;
– random readout of the Output Fifo of the L0 card and of the MD for monitoring purposes.

6 Connections

In Fig. 7 is sketched the ECAL partition in L0 cards for one quarter of calorimeter, and in Fig. 8 the same is shown for HCAL. Under the assumptions of 9U VME crates containing a maximum of 16 L0 cards, and that the right and left halves of the two calorimeters are kept independent,we see that we need 14 9U VME crates to handle 208 L0 ECAL cards and 4 9U VME crates to handle 56 L0 HCAL cards. The L0 trigger electronics is **foreseen to sit on racks placed on top of the mechanical structures of the respective calorimeters**. The L0 calorimeters partition is summarized in

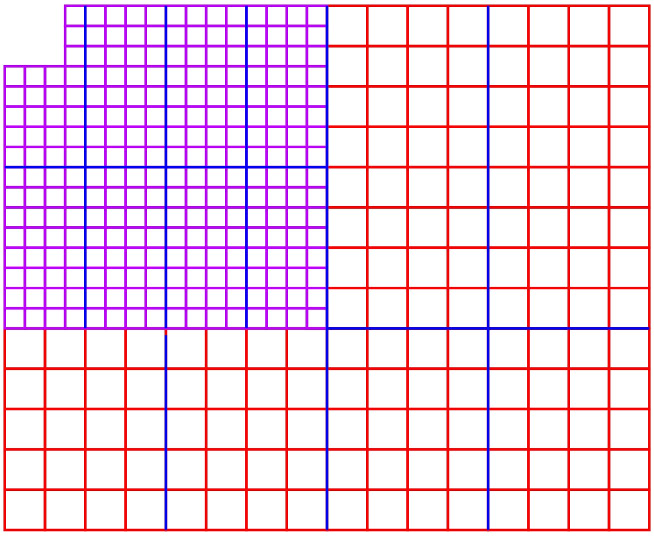

Fig. 8. An HCAL quadrant and its partition in HCAL L0 boards.

ECAL L0 connections for ECAL signals

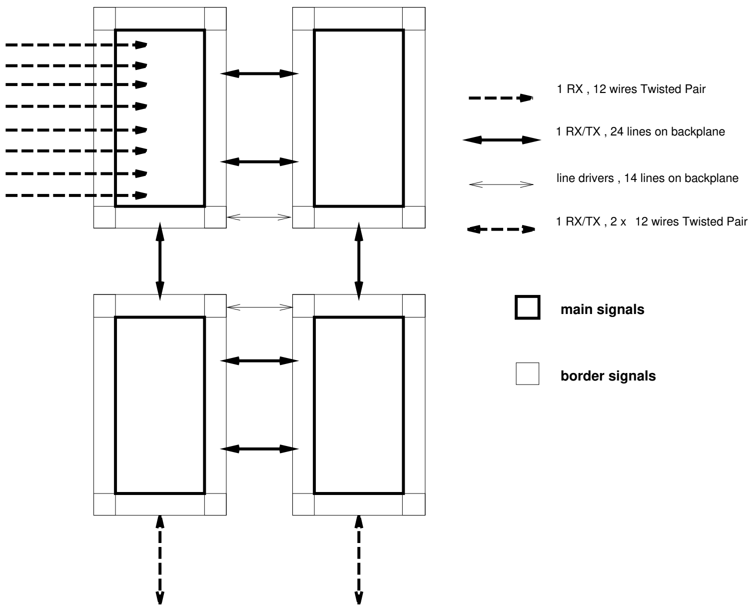

Fig. 9. Schematics view of the connections of the ECAL L0 cards with the ECAL *fed* cards and among the cards themselves to exchange the *borders*.

Table 2. One of the most evident feature of the L0 trigger proposed system is its flexibility in the algorithms which can be performed. This flexibility is achieved at the expense of connections between calorimeters *feds* and the respective L0 cards and between L0 cards themselves.It is clear that once the cost of connections is not an issue anymore (LVDS RX/TX can be used), it remains the problem to minimize the number of cabling. The connections via

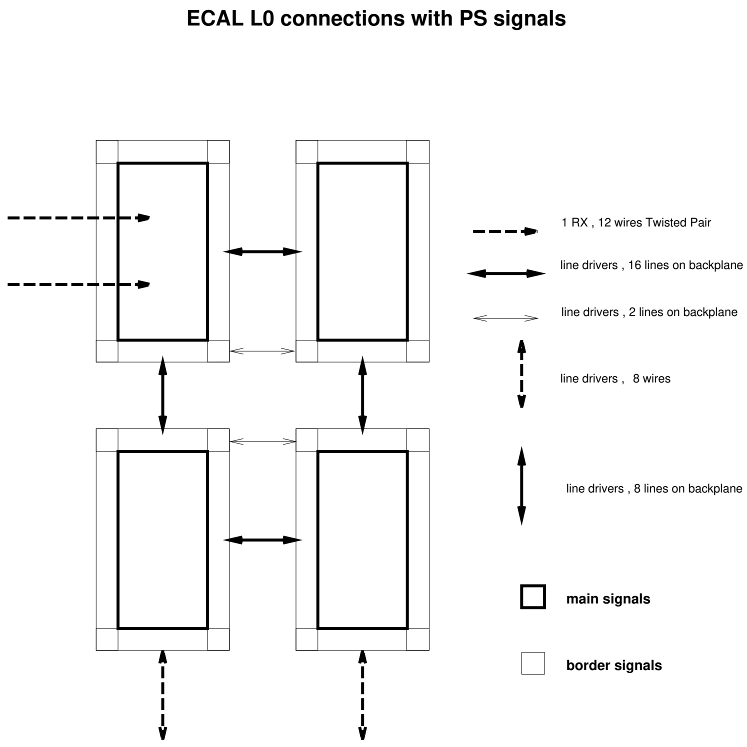

Fig. 10. Schematics view of the connections of the ECAL L0 cards with the PS *fed* cards and among the cards themselves to exchange the *borders*.

Table 2
Summary of 9U VME crates L0 cards.

	9U CRATES	L0 CARDS
INNER ECAL	6	88
OUTER ECAL	8	120
INNER HCAL	2	32
OUTER HCAL	2	24

cable among ECAL,HCAL,PAD and PS *feds* to the respective L0 boards can not be avoided in our design. We will indicate them as $FED \rightarrow L0$ in the following. The connections via cable between the L0 cards themselves , indicated as $L0 \rightarrow L0$ in the following, necessary to transmit the *border* information, can be reduced greatly by using the 9U VME crates backplanes gaining in system reliability.
In the next two subsection we will describe how we intend to realize the above mentioned connections,assuming 28 bit LVDS links which need 12 cable (or backplane) lines.

Table 3
The number of LVDS RX per ECAL L0 card.

	RX per ECAL L0 CARD
ECAL FED $\rightarrow$ ECAL L0	8
PS FED $\rightarrow$ ECAL L0	2
PAD FED $\rightarrow$ ECAL L0	4

Table 4
Description of high-speed links needed for the ECAL and HCAL L0 trigger system.

ITEM	COMMENT	DISTANCE	Q.TY
ECAL FED $\rightarrow$ ECAL L0	28-bit LVDS	10 m	8 x 208
PS FED $\rightarrow$ ECAL L0	28-bit LVDS	10 m	2 x 208
PAD FED $\rightarrow$ ECAL L0	28-bit LVDS	10 m	4 x 208
ECAL L0 $\rightarrow$ ECAL L0	28-bit LVDS	3 m	208
HCAL FED $\rightarrow$ HCAL L0	28-bit LVDS	10 m	8 x 56
ECAL L0 $\rightarrow$ ECAL MD	28-bit LVDS	10 m	4 x 14
HCAL L0 $\rightarrow$ HCAL MD	28-bit LVDS	10 m	2 x 14
ECAL/HCAL MD $\rightarrow$ L0DU	1.5 Gbit/s	70 m	3

6.1 FED $\rightarrow$ L0 connections

The needed number of RX per ECAL L0 card are summerized in Table 3. The relevant numbers can be computed with the help of Fig. 9 and 10. For HCAL we need 8 RX for each L0 board.
In Table 4 we summarize the kind of high-speed involved in the L0 trigger.

6.2 L0 $\rightarrow$ L0 connections

This kind of connections are needed to distribute the *borders* information. The relevant numbers can also in this case be computed with the help of Fig. 9 and 10. Note that to exchange the *border* information we need a couple of RX/TX per board: for each L0 card borders have also to be received.
The "horizontal" borders are exchanged between L0 cards via backplane.
For the "vertical" borders we have to notice that, for instance in the case of ECAL (see FIG. 7), half of the "vertical" connections can be exchanged via backplane since in one crate there are two rows of L0 cards. For HCAL the situation is even more favourable since one crate contains all the boards into

Table 5
Summary of the LVDS RX/TX needed to transmit borders for each ECAL and HCAL L0 card. (h= "horizontal" connections,v="vertical" connections). PAD, PS and "corner" *borders* do not need transmission via RX/TX but simply line drivers and latches.

	RX/TX per ECAL L0 CARD
ECAL borders → ECAL L0	4h + 2v
HCAL borders → HCAL L0	4h + 2v

a partition. For instance all the boards of the HCAL INNER calorimeter (half side) can be fit into one crate.
The border "corners" can be made available via a two step process: first a "vertical" one via a RX/TX LVDS transmission and then an "horizontal" one using fast line drivers and latches. The PAD and PS borders do not need transmission via RX/TX but simply line drivers and latches.
The situation can be summarized in Table 5. For the HCAL L0 cards we need 4 RX/TX for transmission in "horizontal" direction, 2 RX/TX for transmission in "vertical" direction and **no additional cabling** is needed, due to the fact that all the borders can be exchanged via backplane.

7 Cost estimate

In our cost estimate we will assume the following cost for the main components used in our cards:

- FPGA : 250 CHF each;
- 1 Mbyte of RAM [5]: 100 CHF;
- 9U VME crate : 10000 CHF each;
- backplanes : 4000 CHF/crate;

The cost of the high speed LVDS links is not considered,following the general agreement and they're summarised in Table 4. It has to be pointed out that **the cost of FPGAs undergoes strong reduction as a function of time**; nevertheless we assume the 1999 prices for these items. In Table 6 is reported the list of the main components used for each board. The cost of the MD board is guessed to be 6000 CHF. Collecting all these information together and nicely guessing that **the cost of one board is given by the cost of the components times a factor 2.0**, we can summarize in Table 7 the total cost for the whole L0 calorimeters trigger.

[5] The cost of a 32 kbyte fast RAM is about 3 CHF.

Table 6
Description of the main electronic components (and their cost) for the ECAL and HCAL L0 trigger system. The LVDS RX/TX are not included in the cost, following the general agreement.

BOARD TYPE	FPGA	LVDS RX/TX	LUT (Mbyte)	COST (CHF)
ECAL L0 CARD	7	26	0.6	1810
HCAL L0 CARD	5	20	0.5	1300

Table 7
Cost analysis for the whole ECAL and HCAL L0 trigger system. The cost of the L0 cards is obtained **by applying a multiplicative factor 2.0** to the cost of components.

ITEM	UNIT COST (CHF)	Q.TY	TOTAL COST (kCHF)
ECAL L0 CARD	3620	208	753
HCAL L0 CARD	2600	56	146
MESSAGE DISPATCHER	6000	2	12
9U VME CRATES	10000	22	220
BACKPLANES	4000	22	88
TOTAL			1219

8 Milestones

We foresee the following development in order to have the TDR ready for the end of 2001:

- within 1999: Definition of the L0 trigger algorithm. Definition of the details of the design, including, if necessary, HCAL information to the ECAL L0 trigger card. Study of signal transmission.
- End 2000: Full design and simulation of ECAL L0 card
- Mid 2001: Full design and simulation of HCAL L0 card and Message Dispatcher. Prototypes of the ECAL L0 cards available to be tested at CERN or at DESY.
- End 2001: Release of TDR.

9 Acknowledgments

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APPENDIX

A Experimental data available from HERA-B

Here are described some of the experimental data we have from the HERA-B experiment showing the performances that can be obtained at trigger level (with a logic similar to the one proposed in this note for the LHCb L0) on two important points: spatial resolution and capability to detect π^0 signals.

A.1 Spatial resolution at trigger level

During the R&D phase for the design of the HERA-B electromagnetic calorimeter, data were taken at CERN SPS H4 facility. The purpose of these studies was to characterize the HERA-B calorimeter shashlik module as far as concerns the linearity of the response, the energy resolution and the spatial resolution. Among the others, this last point was important to check that the performances of the built modules guarantee an adequate capability to reconstruct em showers impact point both for reconstruction purposes and for trigger purposes. In fact, a good spatial resolution is fundamental in order to reduce the region of interest size (and so the background) for tracks reconstruction at the First Level Trigger.
The test was done on shashlik modules having 5.6 cm side and a depth of 20 r.l..These characteristics are not very different from the ECAL shashlik modules presently considered for the inner part having 4 side and a depth of 25 r.l.. An high energy (from few tens up to 150 GeV) electron beam was impinging perpendicular to the module surface and the position of the impact point was scanned on the surface itself. A wire chamber placed in front of the calorimeter towers measured independently the impact point position of the em shower.
In Fig. A.1 we plot the spatial resolution obtained after correction of the COG algorithm as a function of the impinging electron energy for calorimeter towers having a side of 5.6 cm. The experimental data (open dots) are compared with Monte Carlo simulation. We see a fairly good agreement between real data and Monte Carlo: the spatial resolution obtained by applying a 3x3 cluster COG algorithm is at level of 3 mm for electron energy above 10 GeV.
After processing the data taking into account the simplification due to the algorithm performed by HERA-B pretrigger boards and the effects of the Monte

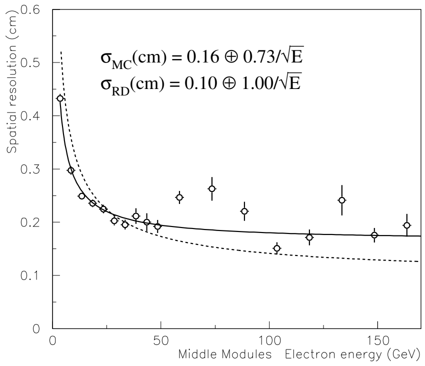


Fig. A.1. Spatial resolutions obtained after COG correction as a function of the energy for modules of cell size 5.6 cm. Dotted line refers to real data and solid one to MC.

Carlo simulated background it comes out that the spatial resolution obtainible at pre-trigger level is about 6 mm.

A.2 Capability to detect π^0 signals at trigger level

One of the most important result obtained up to now by the HERA-B experiment concerning em calorimetry has been to show the possibility to reconstruct clean π^0 signals. This is a very important feature,for instance, for the em calorimeter calibration in standalone mode.
We will not described the criteria on design and on data analysis that led to this important result, but we want to stress the attention on one feature useful for triggering purpose: the capability that the HERA-B experiment has to identify clearly π^0 signals at the very first trigger level. This feature could come out to be useful also in the LHCb experiment, for instance, for **rejecting π^0 background** while triggering on hard photons.
To describe this is worthy to remind that the HERA-B electron pretrigger cards have the capability to store in a pipeline, for monitor purposes, the information that is sent to the tracking system. These pipelines can be readout via VME.
In Fig. A.2 it is shown the invariant mass spectrum calculated from the information collected, at monitor level, from the HERA-B ECAL pre-trigger boards during a recent data taking. The background is evaluated by mixing two different triggered events. A clear π^0 peak emerges from the background. Also interesting is to show that the π^0 peak is evident if we restrict the analysis only to the events, having multiplicity greater than one, belonging to one pre-trigger board (see Fig. A.3).

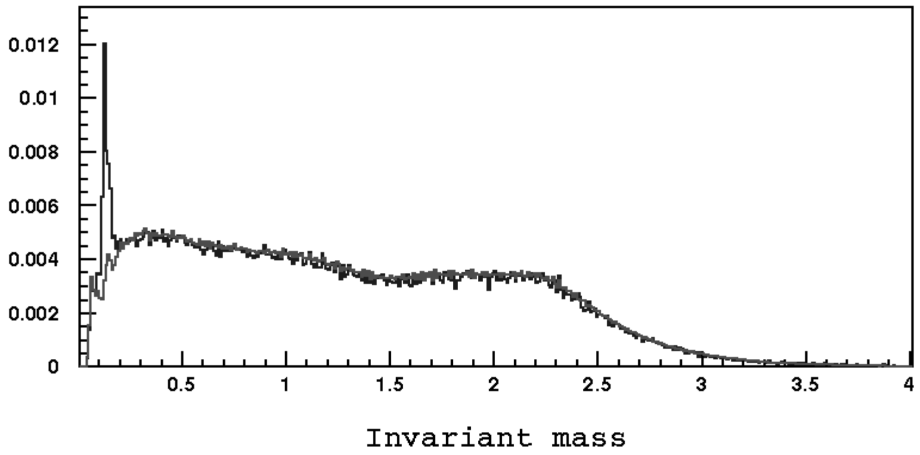


Fig. A.2. Two cluster invariant mass spectrum obtained with the HERA-B ECAL pre-trigger online monitor during a tipical run. Solid line, which is obtained combining same event clusters, shows a nice π^0 signal. Dotted line, obtained by combining clusters of different events, displays the background shape.

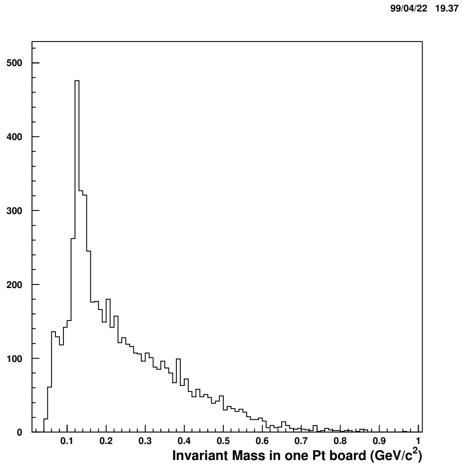
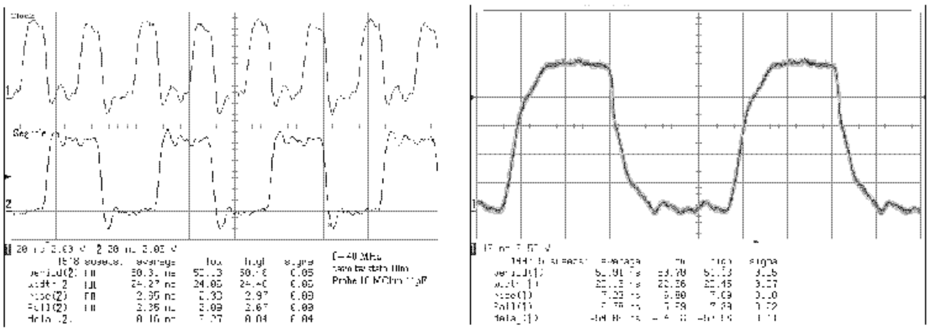


Fig. A.3. Same as Fig. A.2, but the two cluster invariant mass spectrum has been obtained combining candidates of the same pretrigger board.

B Preliminary tests performed on LVDS links

We have performed two kind of tests to check the quality of transmission on normal twisted pair cable using a DS90CR285 transmitter / DS90CR286 receiver pair. In the first test we fed the TX with a clock frequency of 40 MHz and pulse each of the 28 bit with a square wave of half period with respect to the clock and locked with the clock phase itself in order to simulate sequences of "1" (see Fig. B.1 a). Data are transmitted via a normal twisted pair cable (not shielded) long 10 m and terminated on 100 Ω impedance. The received pattern were monitored by means of a mod. LC584A LeCroy Oscilloscope. In Fig. B.1 b) we see the received pattern (one bit line out of 28) on the scope with persistence mode: the received waveform is stable and the measured jitter



a) b)

Fig. B.1. a) The clock and one data bit at the receiver output after 10 meters cable. b) The data bit at the receiver as seen at the scope with the persistance feature activated. The jitter of the reconstructed signal was measured to be 0.8 ns.

is 0.80 ns.

In the second test we fed the TX on all its 28 bit by means of a VME random pattern generator, transmit signals at 40 MHz clock frequency with a cable with the same characteristics described above, receive them by means of a RX and feed them in the input register available in the same VME module. The generated 28 bit patterns can be compared with the received ones: no errors were found after transmission of about 10^6 patterns if the cable was left untouched. Some errors (of the order of few tens over 10^6 transmission) were found if the cable was moved during the transmission itself.

It is clear that the test performed until now can be only be considered **preliminary** (in one second of LHCb there will be of the order of $2 \cdot 10^{11}$ transmissions for the ECAL L0 trigger!) although promising. Tests with other kind of cables (i.e. shielded twisted pairs) and with other connectors are foreseen in order to optimize the signal transmission.

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