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A Joint Proposal for the Level 0 Calorimetric Triggers

Bologna(1) and Orsay(2) LHCb Groups

C.Beigbeder(2), A.Bertin(1), D.Breton(2), M.Bruschi(1), C.Baldanza(1), O.Callot(2), M.Capponi(1), Ph.Cros(2), I.D'Antone(1), S.De Castro(1), R.Doná(1), D.Galli(1), B.Giacobbe(1), B.Jean-Marie(2), J.Lefrançois(2), U.Marconi(1), I.Massa(1), M.Piccinini(1), M.Poli(1), N.Semprini-Cesari(1), R.Spighi(1), S.Vecchi(1), V.Vagnoni(1), I.Videau(2) M.Villa(1), A.Vitale(1), A.Zoccoli(1)

Abstract

In this note we present a joint proposal from the Bologna and Orsay groups to collaborate in building the Level 0 calorimetric triggers for the LHCb experiment. This proposal is the result of many discussions between the two groups during the past months and is based on the ideas described in several LHCb notes ([1], [2], [3], [4], [5]).

The general philosophy and the overall scheme are presented, however the design is far from complete. Work will continue during the coming months to achieve a final design for the Trigger TDR.

[1]Dipartimento di Fisica dell'Università di Bologna and Istituto Nazionale di Fisica Nucleare, Sezione di Bologna
[2]Laboratoire de l'Accélérateur Linéaire (LAL), Orsay

1 Introduction

The present proposal is based on the common philosophy of the two groups, which is to build a **synchronous system** aimed at minimising the number of connections and hardware components. This approach should ensure a robust and cost-effective system with good debugging capabilities.

We believe that the requirements for the *electron* and *photon* triggers are well established, and our understanding of how to implement them is rather advanced. For the *hadron* trigger several new ideas are still under investigation and the final selection of candidates requires more flexibility in the way the final stage of the trigger is implemented.

The note is divided in several sections, which follow the general data flow and its hardware implementation, as displayed in Figure 1:

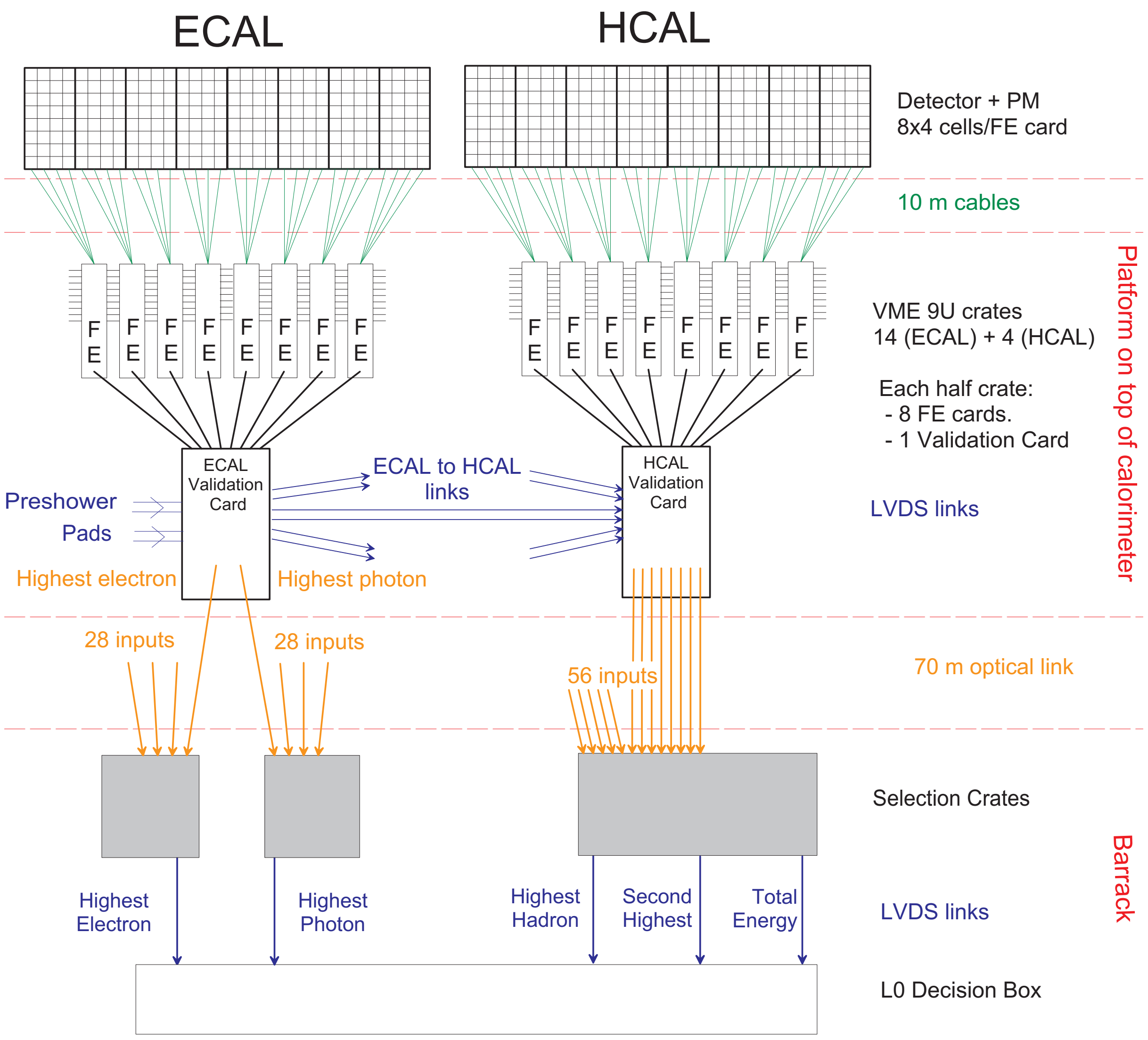

Figure 1: Overall view of the ECAL (left) and HCAL (right) Level 0 triggers

1. A first processing takes place on the front-end boards. Only the candidate with the highest E_T is retained. This step is described in Section 2. It is important to stress that ECAL and HCAL front-end boards are identical in this implementation.

2. A second, validation, step is performed in dedicated *Validation Cards*, located in the front-end crates. This step is detailed in Section 3. ECAL and HCAL Validation Cards are different, since they have to perform rather different functions.

3. The last step is the selection of the final candidates to be sent to the Level 0 Decision Unit. This is done in dedicated *Selection Crates* which are described in Section 4.

In the following, the front-end electronics and the detector geometry correspond to the description given in Ref. [4], which follows the current design of the two calorimeters.

Finally, in the last sections we give rough latency and cost estimates, which still need further studies and we conclude whith a list of milestones which we propose in order to achieve the TDR.

2 Processing on the Front-End Boards

The proposed method is described in [4]. The idea is to select the highest **cluster** in each front-end card, a cluster being the sum of an area of 2x2 calorimeter cells. The input to the trigger system is an 8 bit value obtained from the 12 bit ADC digitization via a look-up table (LUT). The content of this LUT can be defined freely, we call it "E_T" in the following, since a first possibility is the transverse energy in the cell. It has also been proposed to use a bending correction for E_T, and this can be done as long as the formula is valid on a per cell basis, and is additive: The E_T of the cluster is obtained as the sum of the E_T of the four cells.

The advantage of using 2x2 clusters versus 3x3 clusters lies in the reduced number of connections and of operations needed to obtain the parameters of a cluster. The gain is more than a factor 2 in both cases. The 2x2 cluster integrates the shower on a surface less than half the one used in the 3x3 case, and therefore is less sensitive to the underlying event's contribution. It has been shown by simulation, and checked with HERA-B data on 5 cm cells, that the ratio of the energy in the 2x2 over the 3x3 area is around 95 % and has a dispersion of a few %. Using the 2x2 E_T doesn't deteriorate significantly the natural resolution of the calorimeter.

To compute the E_T of the cluster, one needs to access the data of up, up-right and right neighbours, as indicated on Figure 2.

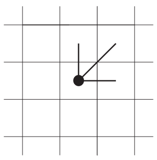

Figure 2: Neighbours of each cell.

A front-end card handles 32 cells, arranged as 8 rows of 4 columns. Most of the neighbours are on the same front-end card, but one needs to access the 4 top cells, the 8 right cells, and the top-right one. The top cells are received via 1-2 meter non-multiplexed links, using shielded twisted pair cables. The 8 right neighbours are received via the backplane. The top-right neighbour is received from the right neighbour card, which receives it from the corresponding top card. The connections between front-end cards are shown schematically on Figure 3.

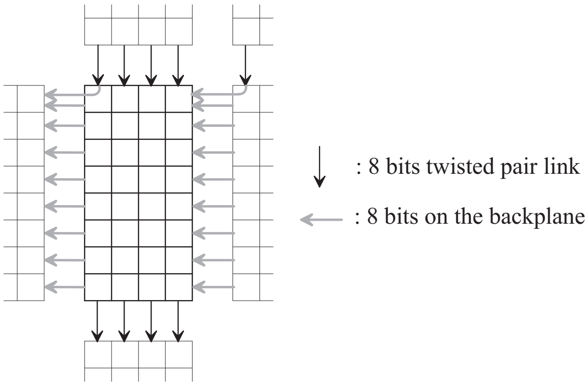

Figure 3: Schematic view of the links between front-end cards. Note the longer path for the neighbour in the 'up-right' corner, which is sent via an up link and then arrives on the backplane.

The first step in the processing is for most of the signals to wait for those arriving from the up card. Then the 2x2 sums are computed in parallel, first performing all the vertical sums of two cells, then all the horizontal ones, keeping the result on 8 bits with saturation at 255 if needed. Next, the highest cluster is selected, by successive comparisons in pipe-line mode: The 32 clusters are compared two by two, producing 16 selected clusters; they are then compared to produce 8, then 4, then 2 and finally, the highest cluster in 5 steps. The output of the cards is the address and the E_T of the highest cluster, and is produced synchronously with a fixed latency of 8 clock cycles: 1 clock cycle to wait for the up neighbours, 2 to compute the vertical and horizontal sums and 5 to select the highest.

A schematic view of the connections needed on a front-end card is shown on Figure 4.

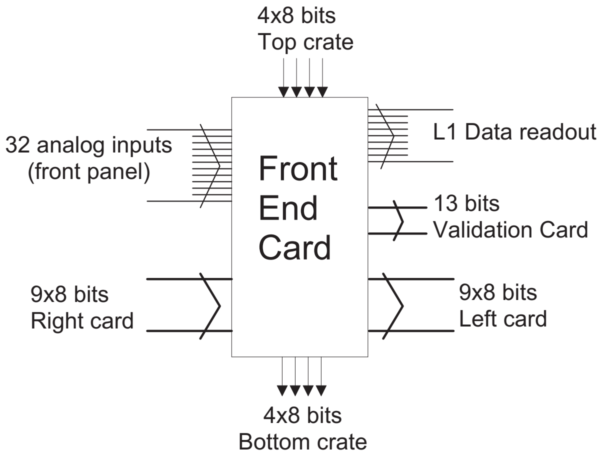

Figure 4: Schematic view of the connections on a front-end card

The position of the selected cluster is defined by its (bottom left) cell number. The accuracy with which one knows the position is about half a cell: if the shower is not close to the center of the 2x2 area, then another 2x2 area would have been selected as highest. If a better accuracy is required for the Level 1 trigger system, it is possible to compute a more accurate estimation of the shower position. One has to keep, during the selection process, the E_T of the 4 individual cells, which means a longer 'word' to transport, but the same operation for summing and selecting. Once the highest cluster is selected, one performs the sums of the two columns and two rows. Finally, these sums are presented to two look-up tables to obtain an estimation of the center of gravity coordinates, one LUT gives X from the columns, the other gives Y from the rows. Although this more precise position estimate is possible, it has a non negligible cost, and since the need for it is not yet clearly established, this option is not part of the baseline proposal.

3 Validation of the Candidates

The validation is performed differently for ECAL and HCAL. But the basic scheme is similar: Each VME crate contains two Validation Cards, each of them handling 8 Front-End cards. The cluster information is on 13 bits (8 bits E_T, 5 bits address) received via the backplane. Input from other detectors is used to validate the 8 clusters, and to produce candidates, to be sent to the Selection Crates by optical links. The candidates information is on 29 bits: 8 bits E_T, 13 bits address and 8 bits BX-id.

3.1 ECAL Validation Card

The ECAL Validation Cards handle 8 rows and 32 columns, an horizontal slice in the calorimeter. The inputs are:

- 8 clusters from the 8 Front-End cards.
- 9x32 bits from the corresponding area of the Preshower.
- 9x33 bits from the Pad detector. Each bit is the OR of two physical pads of the MU1 chamber.

The validation for the electromagnetic nature of the selected clusters and the electron and photon signatures proceed as described in [4]. A cluster which is not electromagnetic is not considered as a candidate and ignored (zeroed) in the following.

The output of the Validation Card is then from 0 to 8 photon and from 0 to 8 electron candidates. As we want to obtain only the highest E_T electron and the highest E_T photon, we intend to select the highest of the 8 on the card, to minimize the number of long distance links. Even if this functionality is part of the selection mechanism, it is better to implement it on this Validation card.

This card sends also the 8 input ECAL clusters to one HCAL Validation Card. The geometry is such that we don't need to send the same ECAL cluster to two different HCAL cards. We have then 208 LVDS links between the two detectors.

3.2 HCAL Validation Card

The HCAL Validation Card has for only function to add the ECAL energy in front of each HCAL cluster, and to send the result to the Selection Crate. For each HCAL Front-End card, only a small number of ECAL clusters, one, four or nine, can be in front. The matching of the addresses is performed via look-up tables, with 5+5 address lines. Then the matching candidates are compared, and the highest E_T selected, and finally added to the HCAL cluster. The whole operation takes 6 cycles: One to match, 4 to select the highest, and one to add.

4 Final Selection

The purpose of the Final Selection logic block is to provide the L0 decision unit with:

- highest E_T electron;
- highest E_T photon;
- highest E_T hadron;
- second highest E_T hadron;
- Total E_T;

The search of the highest E_T electron (photon) candidate could be done in one step process: the 28 candidates obtained from the validation could be sent to an ECAL Electron (Photon) Final Selection board handling 28 candidates. The latency for this step is 5 clock cycles.

The highest E_T hadron can be produced the same way the highest E_T electron and photon are selected. But we will probably want also the second highest E_T candidate and for this operation a "ghost" cleaning is needed in the sample of candidates provided by the HCAL Front-End boards. These operations ("ghost cleaning" and search of the second highest E_T) can be performed with the logic block derived from Ref. [5] and shown in Fig. 5.

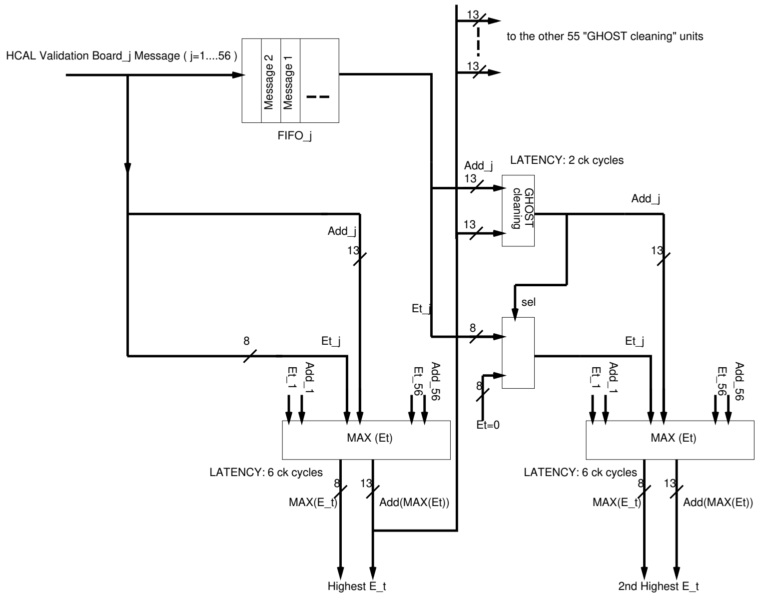

Figure 5: The logic block to select the second highest E_T candidate for the HCAL L0 trigger. This block provides also a "ghost" cleaning.

The candidates from HCAL are processed in pipe-line in two independent sections, one providing the highest and the other one providing the second highest E_T candidate. One FIFO at the input of the second section ensures the correct time alignment between the operations. The first section searches for the address and the value of the highest E_T candidate. The address of the found candidate is used to mask, by means of the "ghost cleaning" logic block , the addresses of the candidate itself and of the "ghosts" in the search for the second highest E_T candidate.

The ghost cleaning is based on comparison of the address of the clusters: Two clusters are ghosts if they share a cell, which means that their address both in X and Y differs by 0 or ± 1, and are in the same calorimeter region. This criteria allows to remove the highest E_T candidate and all its ghosts with a simple logic on the addresses. By "remove" we mean replacing E_T by zero for this cluster. The selection of the highest of the remaining clusters produces the second highest E_T hadron.

This selection takes 6 cycles for finding the highest E_T candidate, 2 cycles for the ghost cleaning, and another 6 cycles for finding the second highest.

One can also compute the total E_T by adding the 56 E_T together if it's shown to be useful either for pile-up veto or to enrich in B events.

The overall L0 calorimeter system is completely synchronous. A logic can be developed in the Validation and Final Selection blocks that checks the consistency of the BX id coming from the different parts of the system and eventually adds an error bit to the candidate in the case a fault is detected.

5 Latency

The processing time needed for each of the trigger steps is explained in the relevant sections. As mentioned previously, we propose to have the selection crates located in the barracks close to the Level 0 Decision Unit. Table 1 summarises the time taken from the availability of the data in the FE card to the reception by the Level 0 Decision Unit.

Step	Nb of cycles	source of delay	delay (ns)
Processing in FE card	8		200
Validation	4 + synchro		150
Sending to Selection Crate		70m + drivers	450
Selection	< 20		< 500
Sending to Level 0		10m	50
Total			< 1350

Table 1: Latency for the calorimetric Level 0 trigger t_{calo}

6 Cost estimate

The cost estimate presented in this section is based on 1999 prices for existing or announced commercial components. No spares are included in the cost.

Since part of the trigger hardware is integrated on the front-end electronics boards, we have counted the cost of the specific components, and separately the fraction of the cost of the PC board used for these components. The short-distance links between the front-end boards of different crates (Fig. 3) are included in the cost as well as the price of the specific backplane connections. The Validation Cards are included in their totality. The cost of the specific part of the backplane is given, as well as an appropriate fraction of the cost of the crates. The results of this exercise are given in Table 2.

The high-speed links have been identified, their length and band-width are summarised in Table 3. No cost estimate is attempted, according to the general agreement.

Item	unit cost CHF	quantity	Total cost kCHF
(Trigger part of front-end boards			
Hardware components	640	248	160
10% of the PC board	50	248	12
ECAL Validation Card	4000	28	112
HCAL Validation Card	4000	8	32
25% of front-end backplane	250	18	5
9U VME Selection crates and backplane	13000	2	26
ECAL Selection cards			50
HCAL Selection cards			50
Total			447

Table 2: Cost estimate for the hardware components of the Level 0 Trigger

Item	Comment	distance	quantity
Preshower links to Validation Card	9-bit LVDS	10 m	32 x 28
Pad chamber links to Validation Card	9-bit LVDS	10 m	33 x 28
ECAL to HCAL links	13-bit LVDS	10 m	208
Validation Card to Selection Crates	1 Gbit/s optical	70 m	2 x 28 + 56
Selection crates to Level 0 Decision Unit	32 bits LVDS	5 m	5

Table 3: High-speed links involved in the Level 0 trigger

7 Milestones

It is clear that a lot of work is needed to convert this proposal to a TDR. We foresee the following scenario:

- Summer 1999: A prototype front-end card is built for the calorimeter test beam. Although this card will not have the trigger part implemented for the test beam, the possibility is provided to add this part later, for tests in the lab which will take place during the fall.
- End 1999: A complete design of the calorimeter front-end card will be available. The design will include the trigger part, as described in this note. The details on the test and monitoring sub-systems may be finalised later.
- End 1999: A first technical description of the Selection Crates is available.
- Mid 2000: A complete design of the two Validation Cards, ECAL and HCAL, will be available. The exact date depends on the choice of the Pad Detector, and on the progress in the design of the Preshower front-end card.

- End 2000: The Selection Crates are fully specified and a complete design is available.
- Mid 2001: A description of the methods and tools for testing the various cards is released.
- End 2001: Release of the TDR

The above does not represent a detailed work plan, rather it is meant to provide a reasonable estimate of the order of priorities. Work will also continue in parallel on the simulation of the trigger in the LHCb Monte-Carlo, to try to improve it's performance before the design is frozen.

8 Conclusion

This joint proposal provides a synchronous calorimeter trigger to LHCb. The system is economical, as it requires only a small modification of the FE cards, two extra cards per front-end crate, two extra crates in the barrack for the final selection, and a reasonably small number of links. The design has to be pursued, but the two groups are working together and have enough strength to design, build and operate this system.

References

[1] D.Breton et al, 'An Alternative High p_T Electron Trigger for LHC-B'
LHCB 97-021 (3 December 1997)

[2] The LHCb Bologna Group, 'The HERA-B electromagnetic pre-trigger and its possible adaptations to the LHCb Level-0 calorimeter trigger'
LHCb 98-034 (10 February 1998)

[3] The LAL LHCb group, 'An Alternative High $\mathrm{P_T}$ Electron and Hadron Trigger for LHCb'
LHCb 98-058 (4 September 1998)

[4] C.Beigbeder et al, 'An Update of the 2x2 Implementation for the Level 0 calorimeter Triggers'
LHCb 99-007 (29 April 1999)

[5] The LHCb Bologna Group, 'Proposal for a Level 0 calorimeter trigger system for LHCb'
LHCb 99-013 (May 1999)