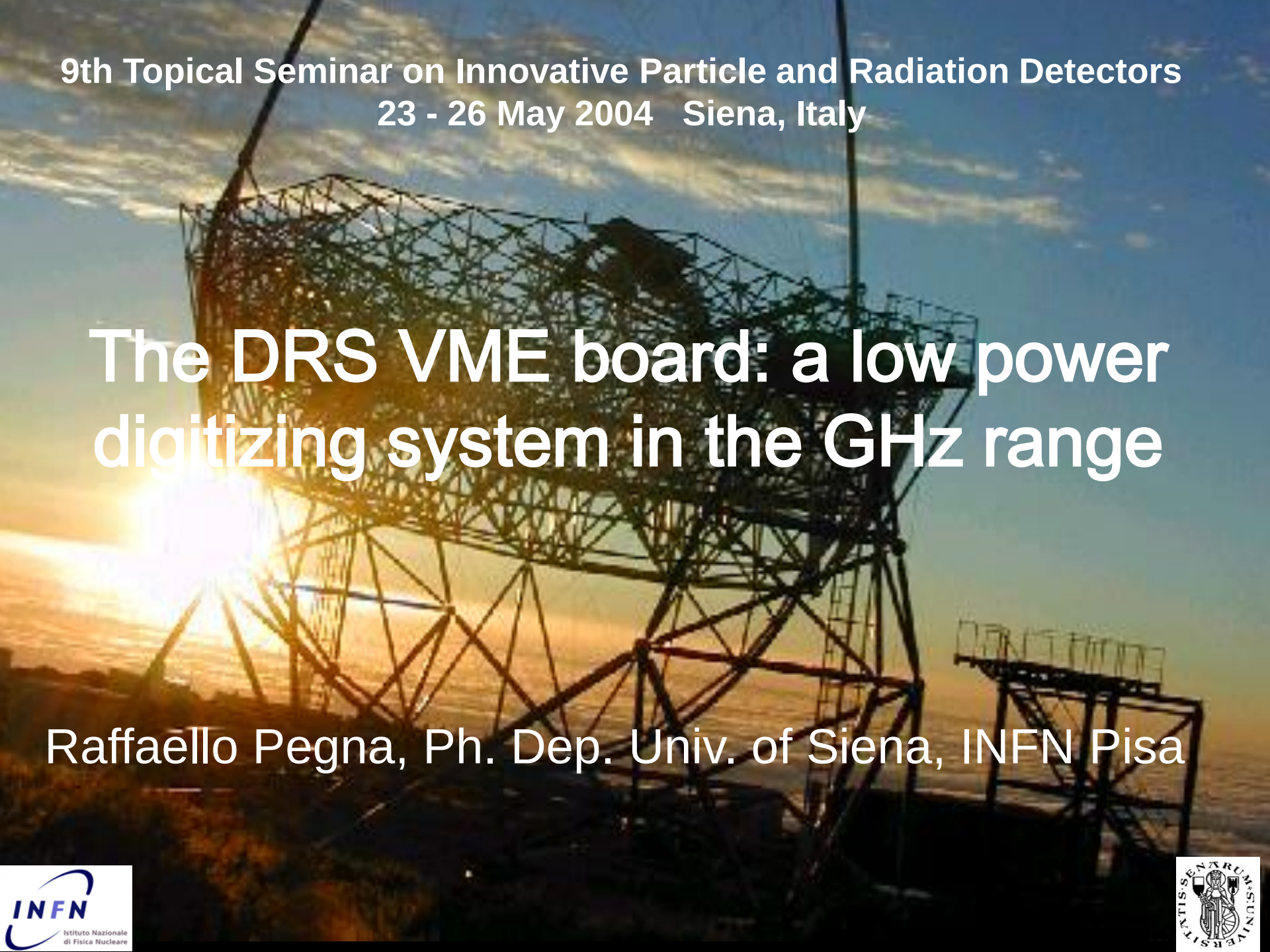


9th Topical Seminar on Innovative Particle and Radiation Detectors
23 - 26 May 2004 Siena, Italy

The DRS VME board: a low power digitizing system in the GHz range

Raffaello Pegna, Ph. Dep. Univ. of Siena, INFN Pisa

The MAGIC Telescope

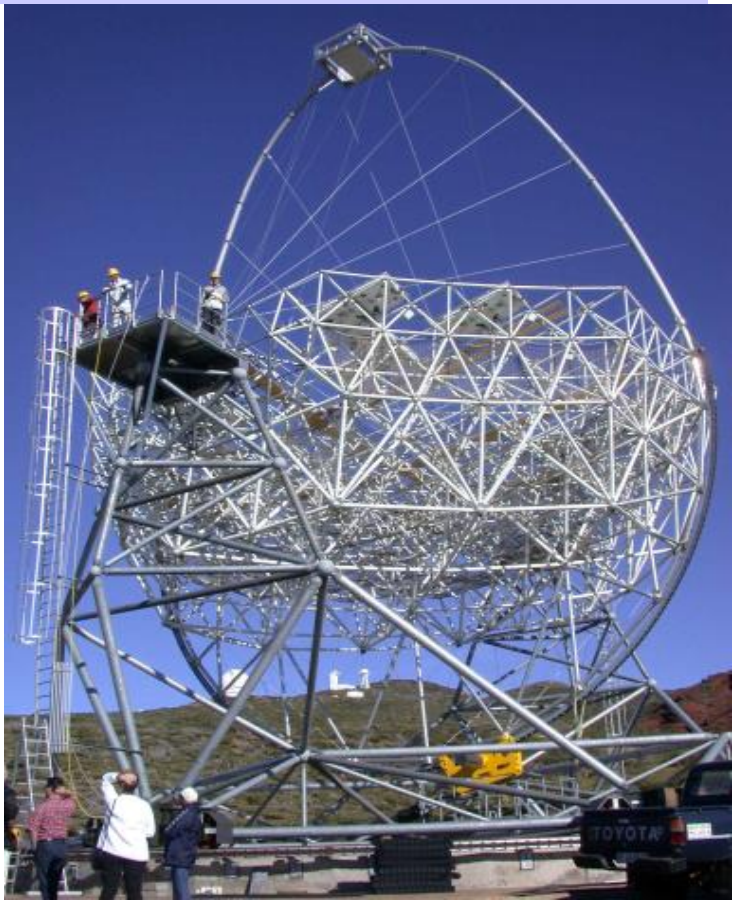
Major Atmospheric Gamma-Ray Imaging Cherenkov Telescope

Barcelona IFAE, Barcelona UAB, Crimean Observatory, U.C. Davis, U. Lodz, UCM Madrid, INR Moscow, MPI Munich, INFN/ U. Padua, **INFN/ U. Siena** U. Siegen Tuorla Observatory, Yerevan Phys. Institute, U. Wuerzburg

Main aim: to detect γ-ray sources in the unexplored energy range from 30 to 250 GeV

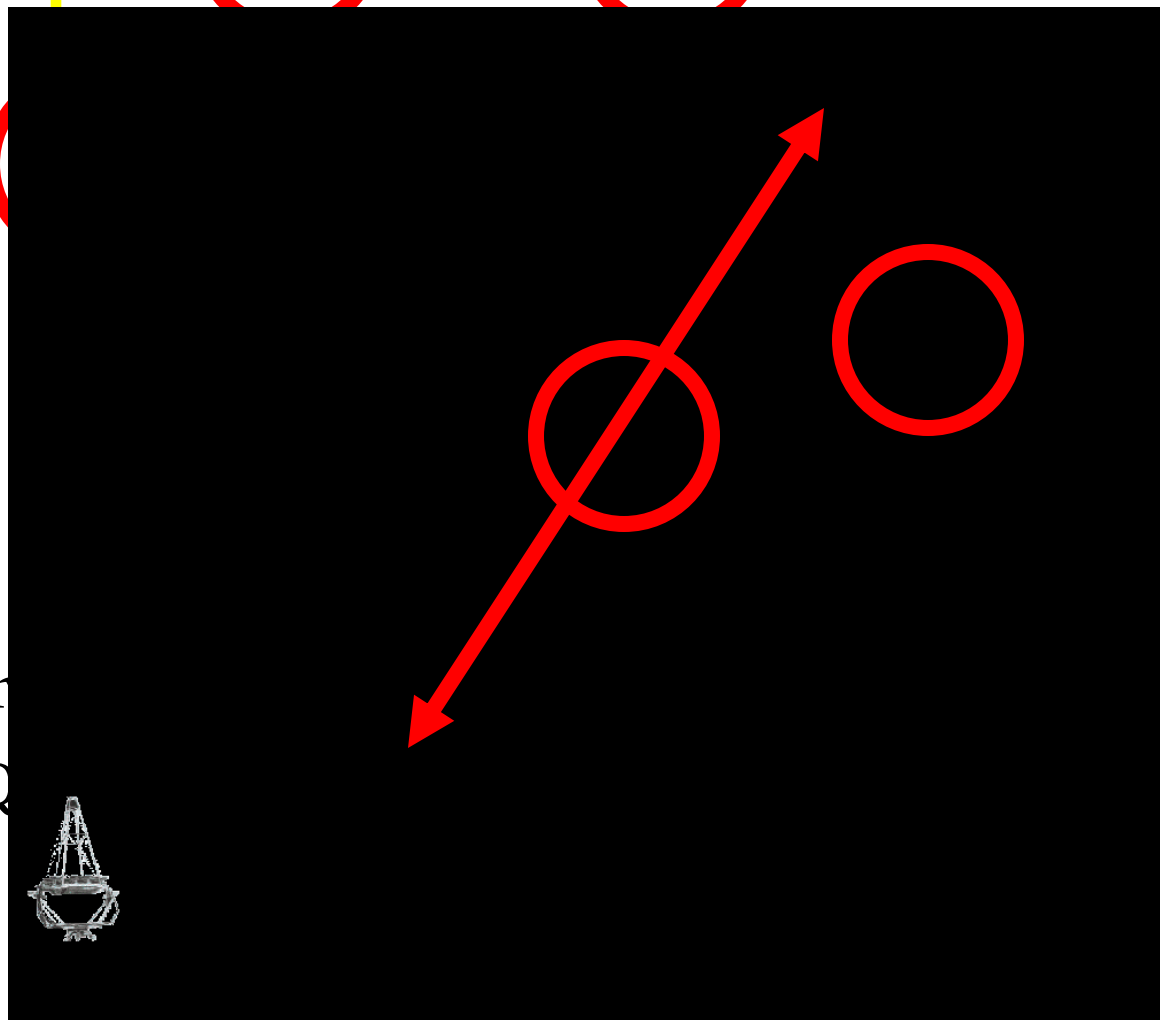
Magic needs a challenging design to decrease the energy thresold, pushing the affordable technology in terms of mirror size, trigger, camera and electronics.

Magic will have the lowest energy thresold ever obtained whit a Cherenkov telescope.



MAGIC telescope concept

- 17 m diameter dish
- Ultra light carbon fibre frame
- Active mirror control
- 577 PMT pixels, 3.9 deg FOV camera
- Optical signal transpor and FADC based DAQ
- 2 level trigger system



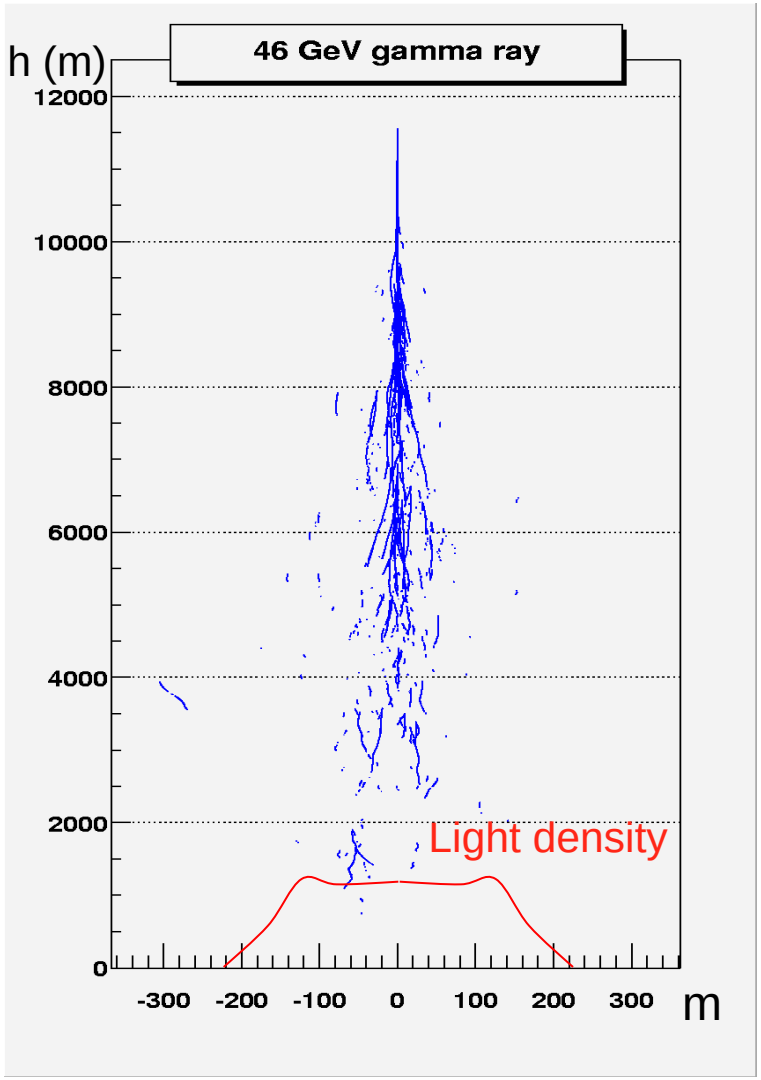
Extensive air showers

Gamma rays initiate showers of charged particles ($e^{\pm}$) on entering the atmosphere

High energy $e^{\pm}$ ($v > c/n$) emit Cherenkov light which reaches ground level as a short flash (≈ 3 ns)

High background rate due to hadronic showers.

Light contamination from NSB, moon, stars.



Noise rejection techniques

Online: next neigbours tight time coincidence (NSB, L1) and advanced pattern recognition (γ/h, L2).

Offline: pmt pulse shape and timing analysis (fast waveform recording)

Lowering the Energy Threshold

$$E \propto \sqrt{\frac{\phi \Omega \tau}{A \epsilon}}$$

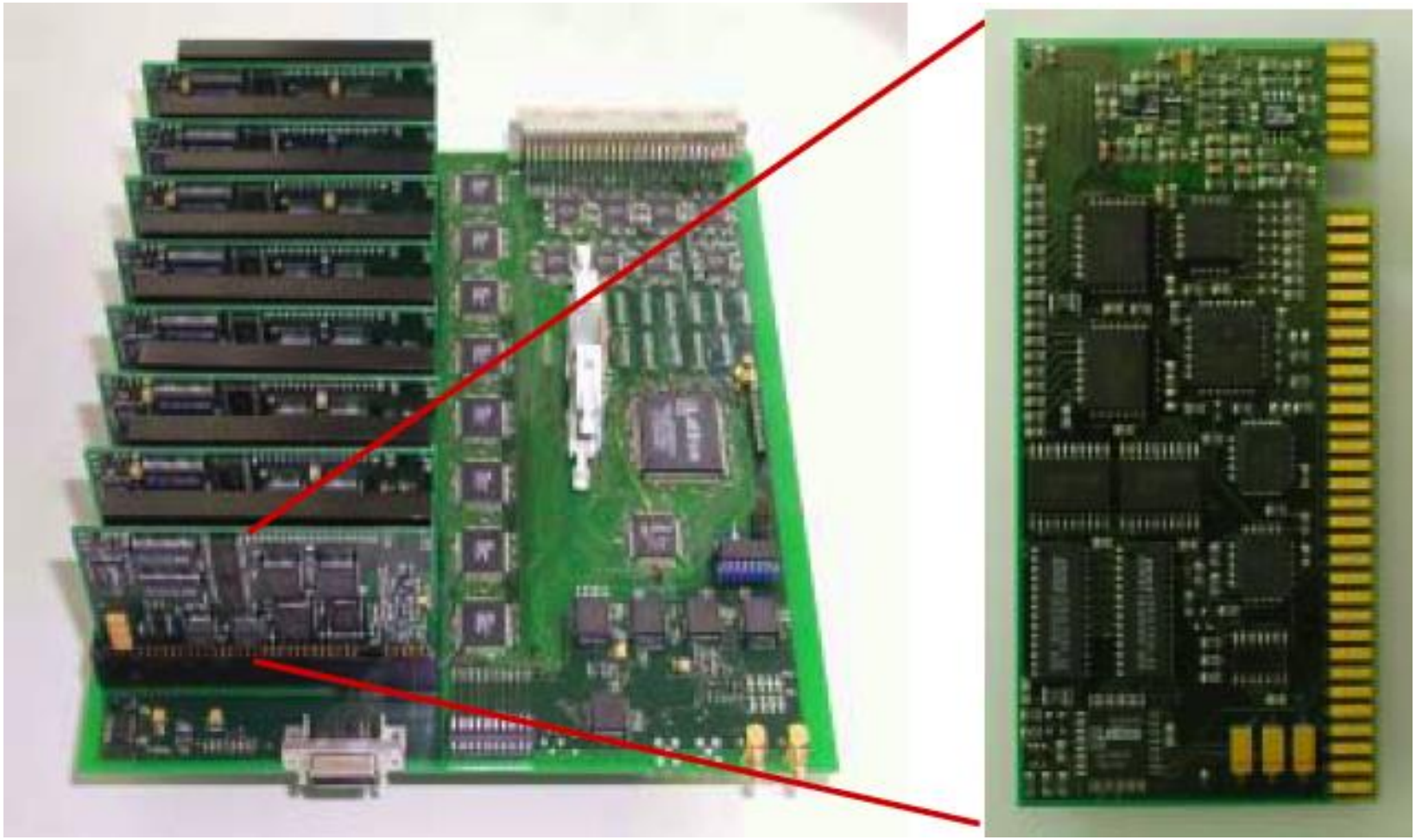
Ω - Pixel Solid Angle

τ - Integration time

A - Mirror Area

ε - Quantum Efficiency

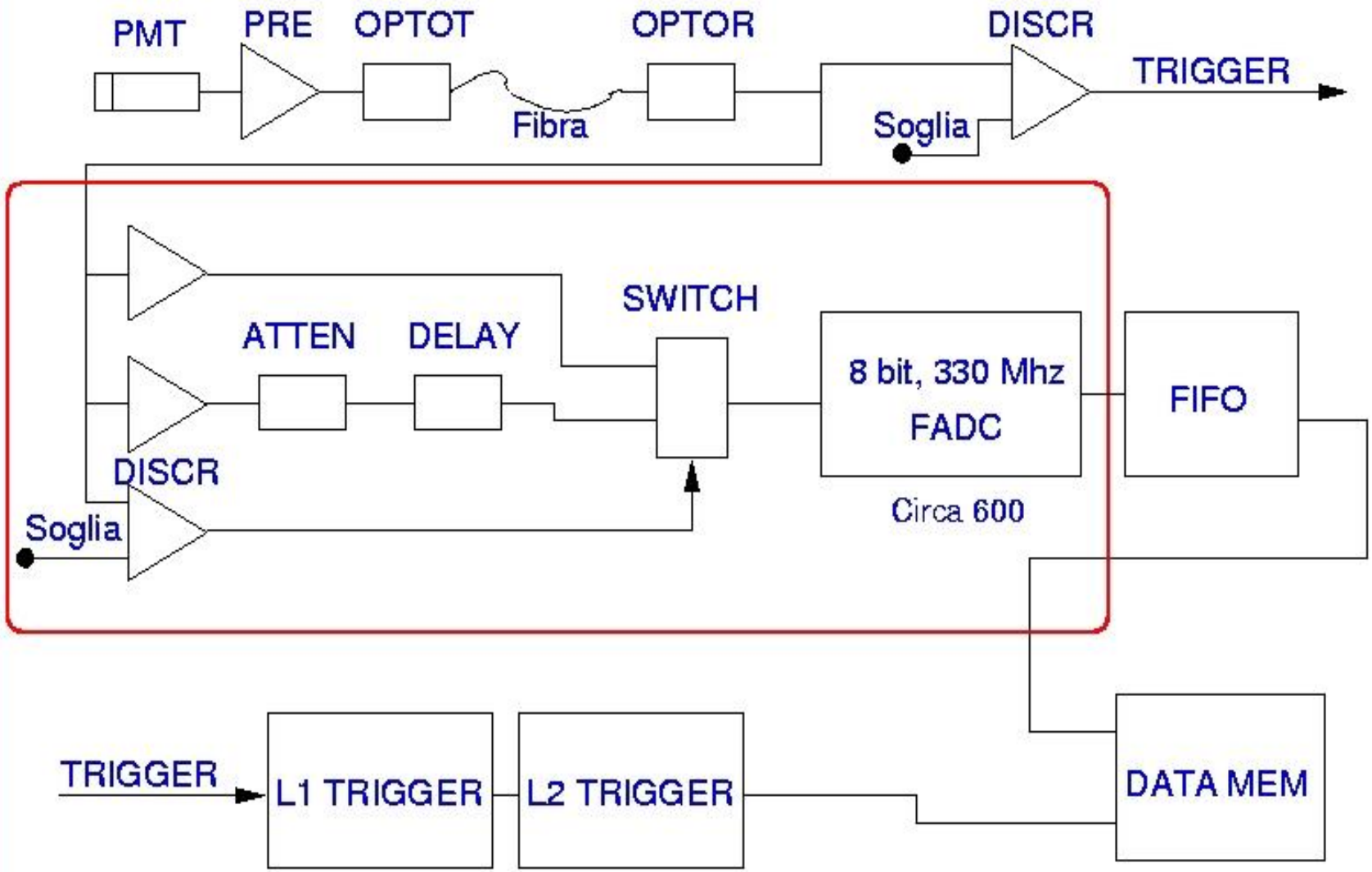
Flash ADC @ 330 MHz, 8 bit



High/Low gain channels

~5 W/channel

The DAQ of MAGIC

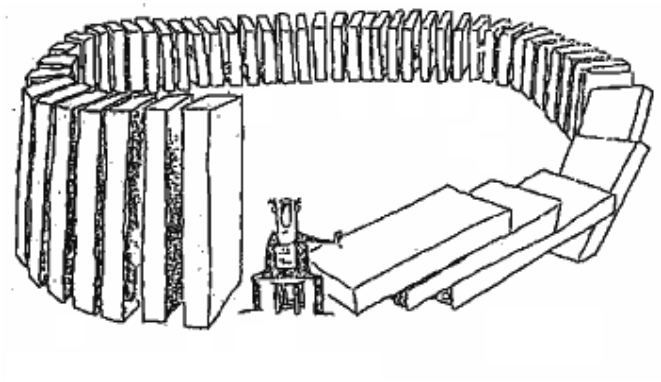


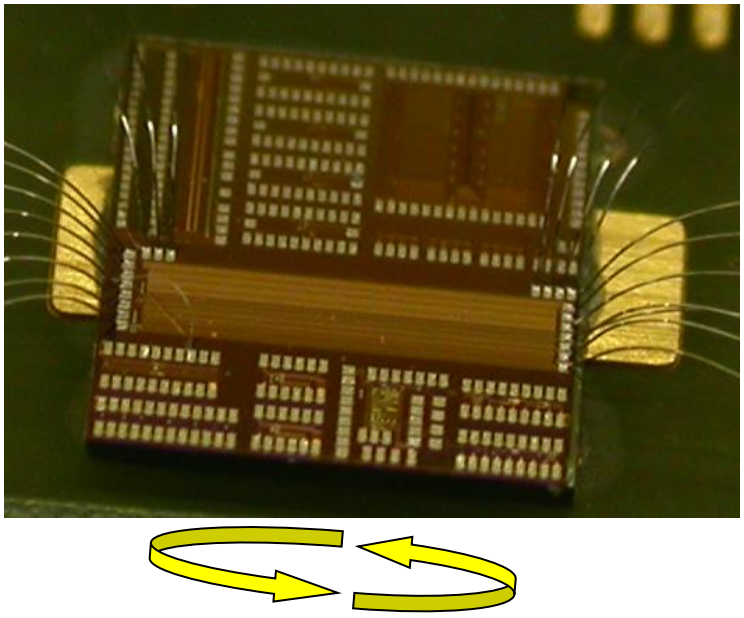
The DRS Chip

Developed by Stefan Ritt, Paul Scherrer Institute, Switzerland for the MEG ($\mu^+ \rightarrow e^+ \gamma$) Experiment

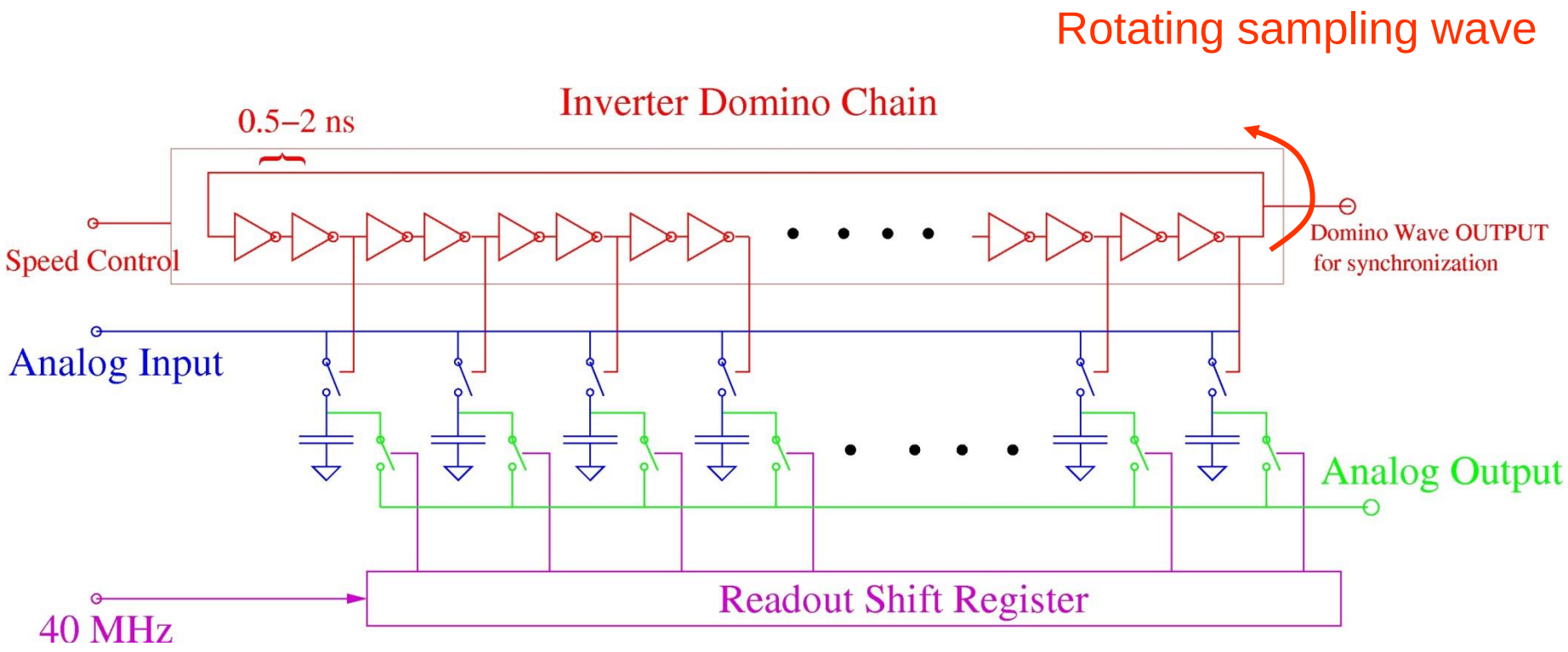
0.25 μm CMOS Process

"DOMINO RING SAMPLER"

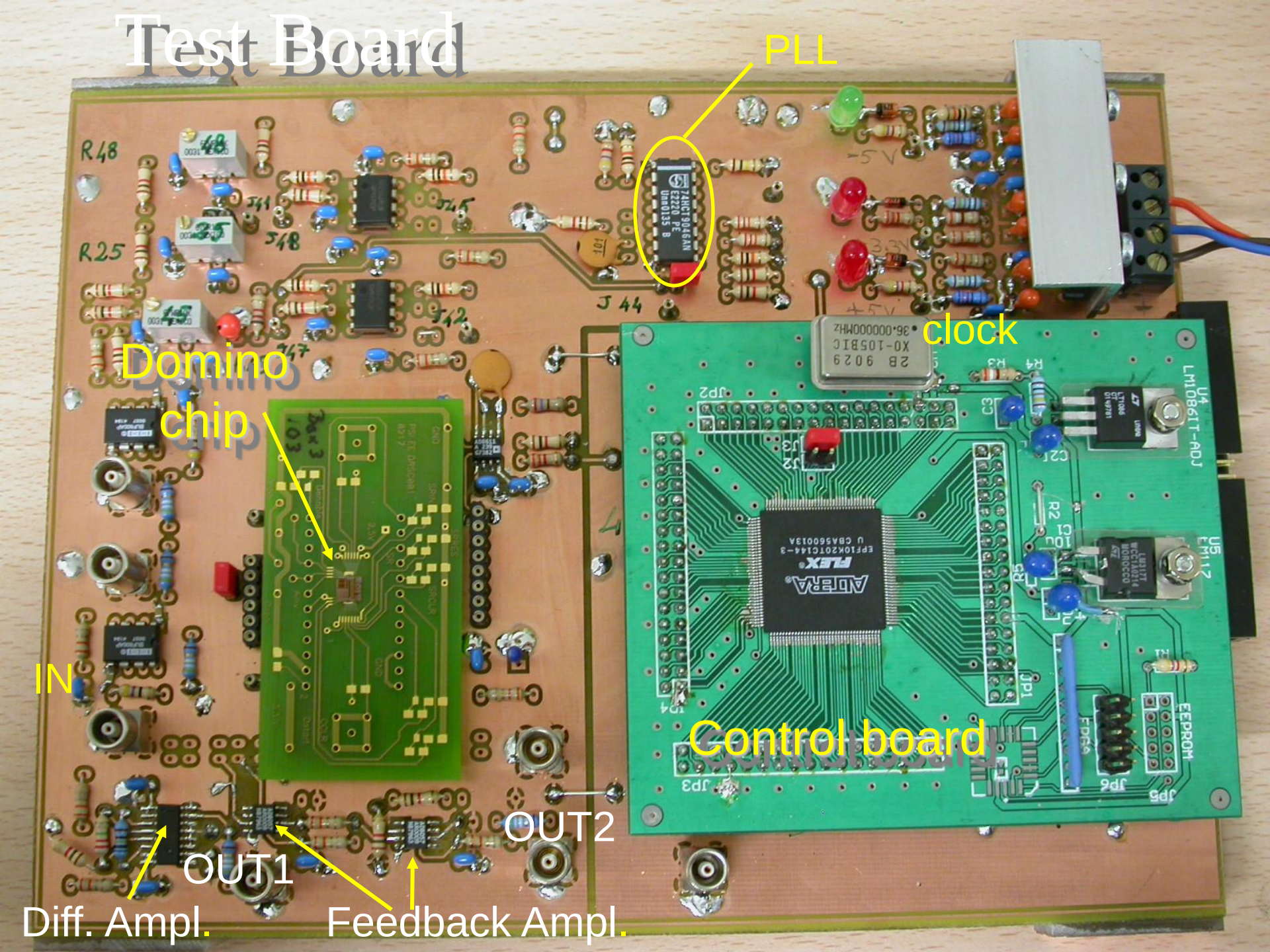




Simplified DRS circuit diagram

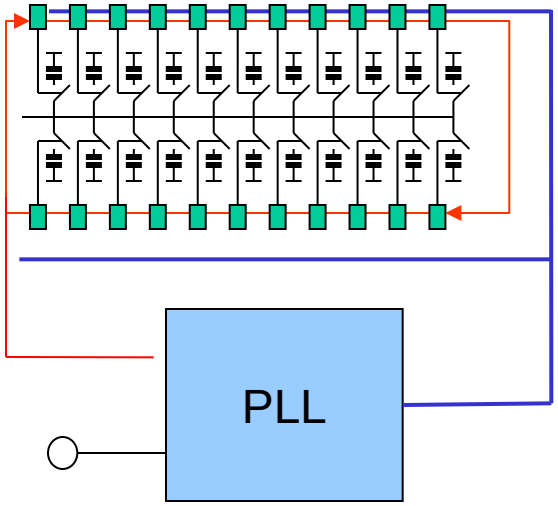


- Freely propagating rotating sampling signal
- Fast **Analog** sampling in an array of capacitors
- Slow 40 MHz readout of the stored signal and external digitization


Test Board
PLL
clock
Domino chip
IN
Control board
OUT2
OUT1
Diff. Ampl.
Feedback Ampl.

Faced Problems

1) Domino Wave sinchronisation



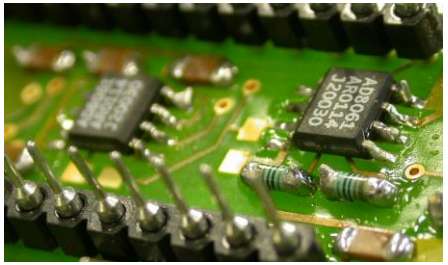
Design of a PLL

sistem to lock the sampling

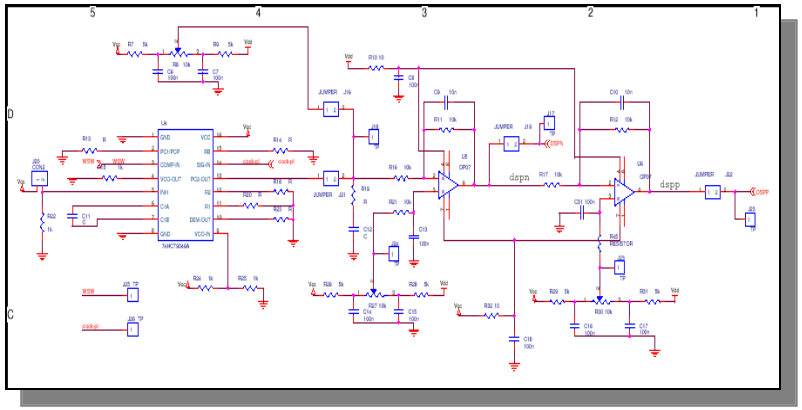
wave to an external clock

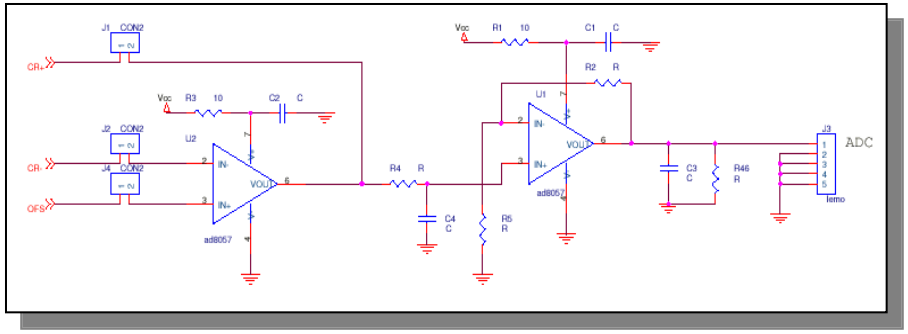
External
Common
Reference Clock

2) Output signal amplification & readout

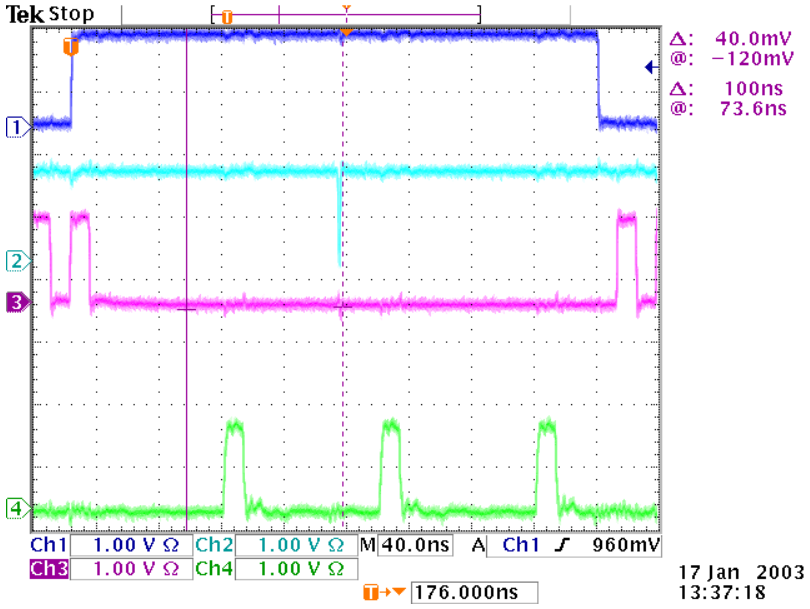


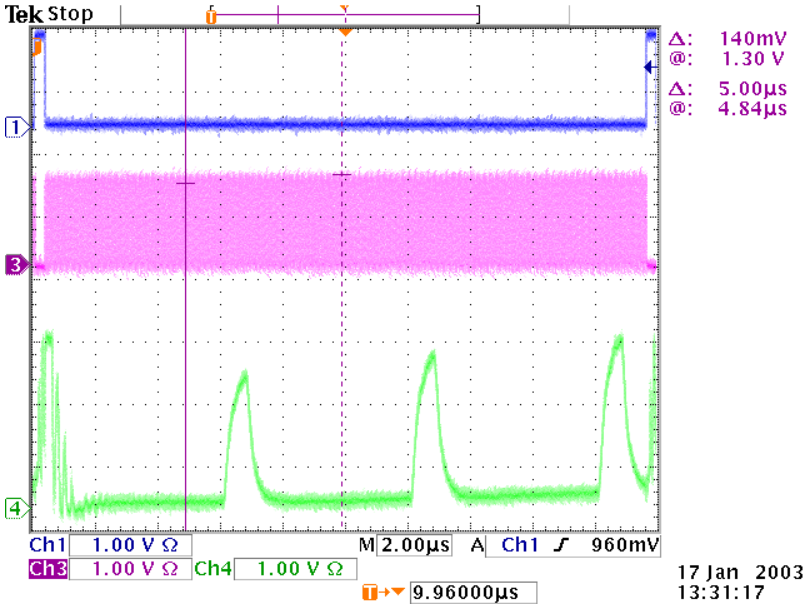
Amplification of the suppressed output signal

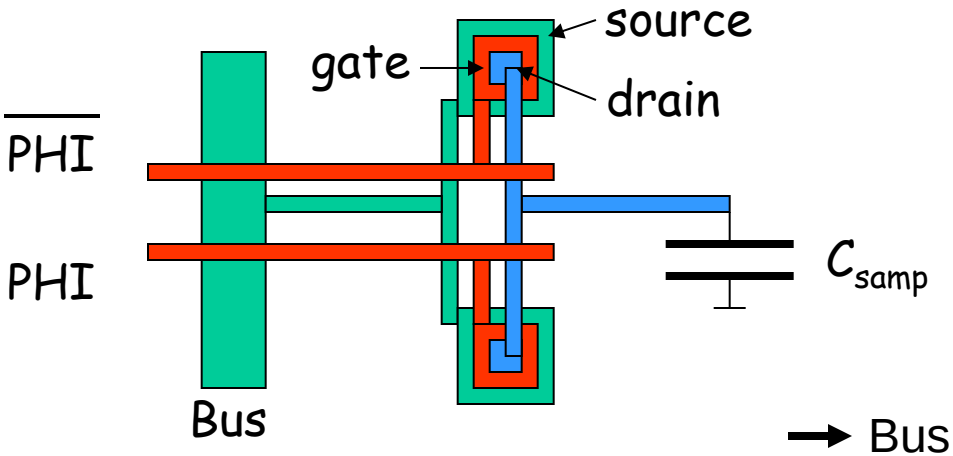




Problems in DRS1 analog part





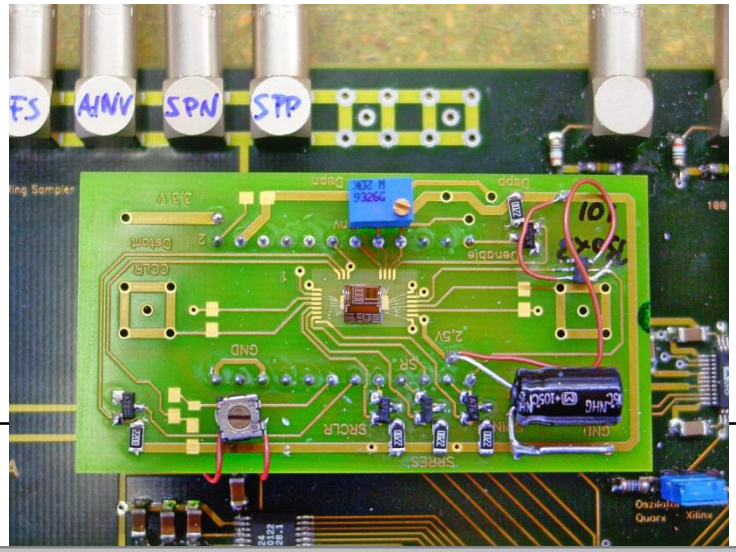


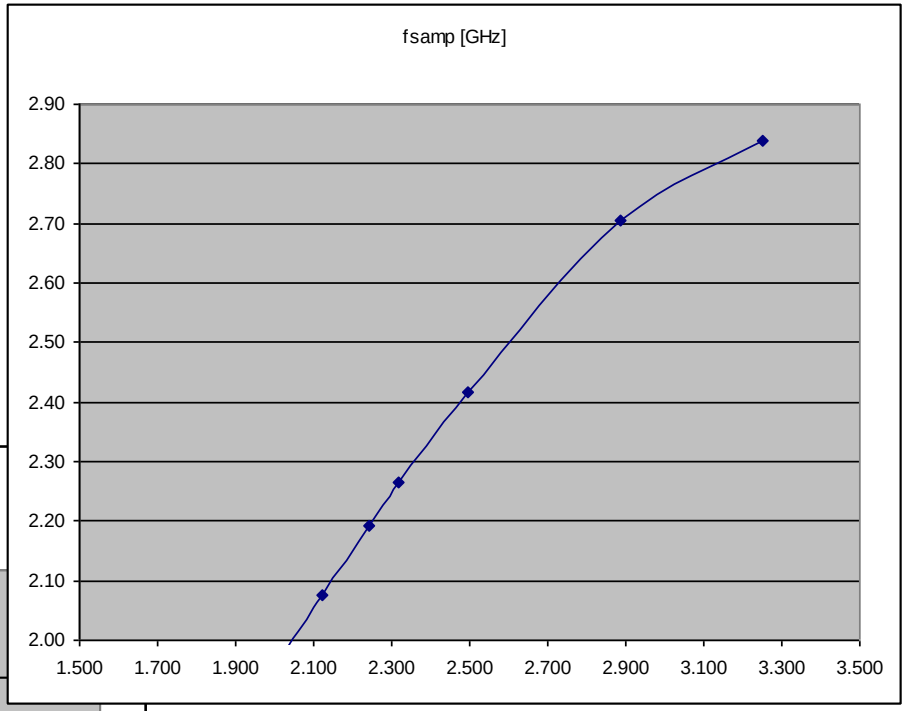
Capacitances:

Gate-Bulk:	10.6 fF
Source-Bulk:	13.5 fF
Drain-Bulk:	2.4 fF
C_{samp}:	200 fF

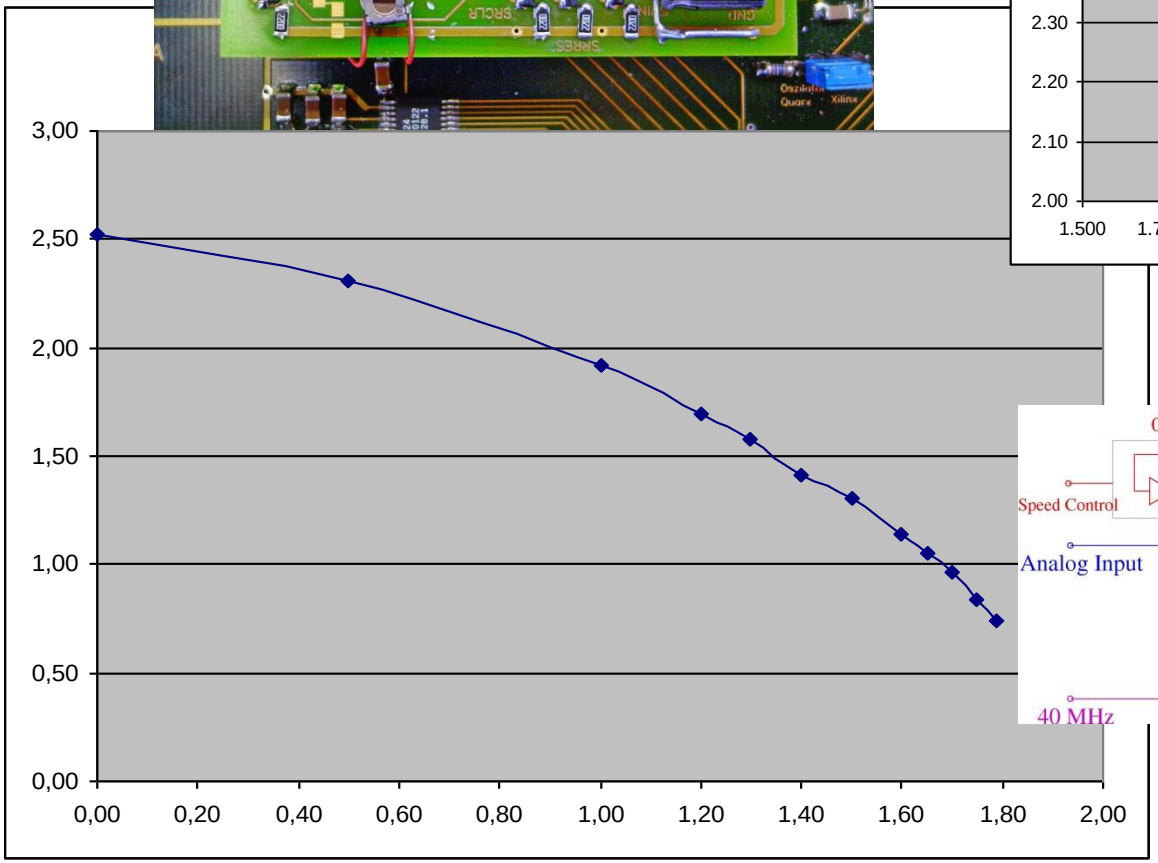
→ Bus capacitance too high (110pF)

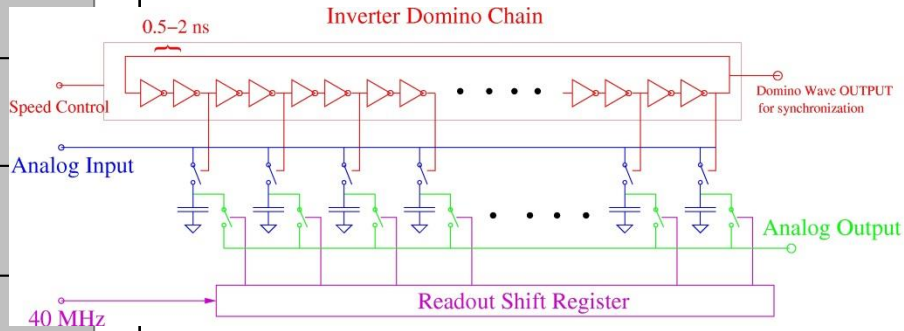
Domino1 “VCO” measurements





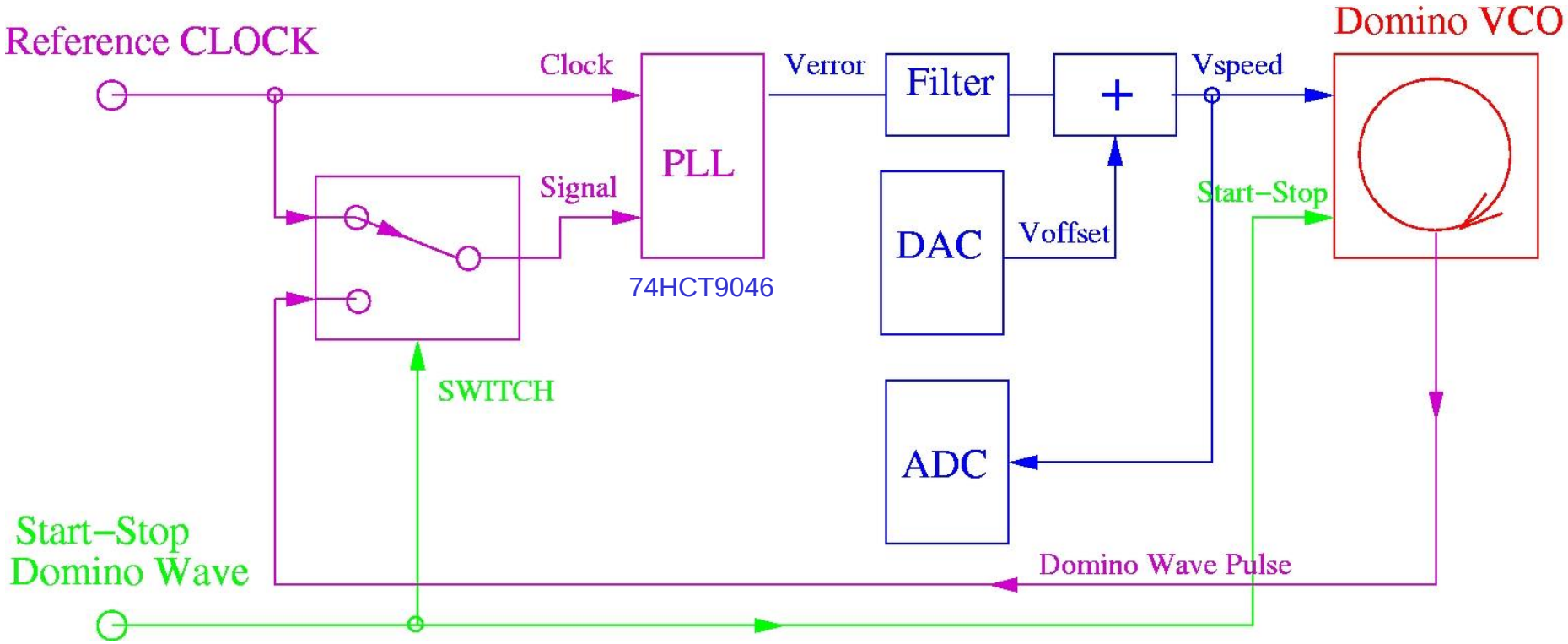
$f_{samp}[GHz]$ vs. $V_{dd}[V]$





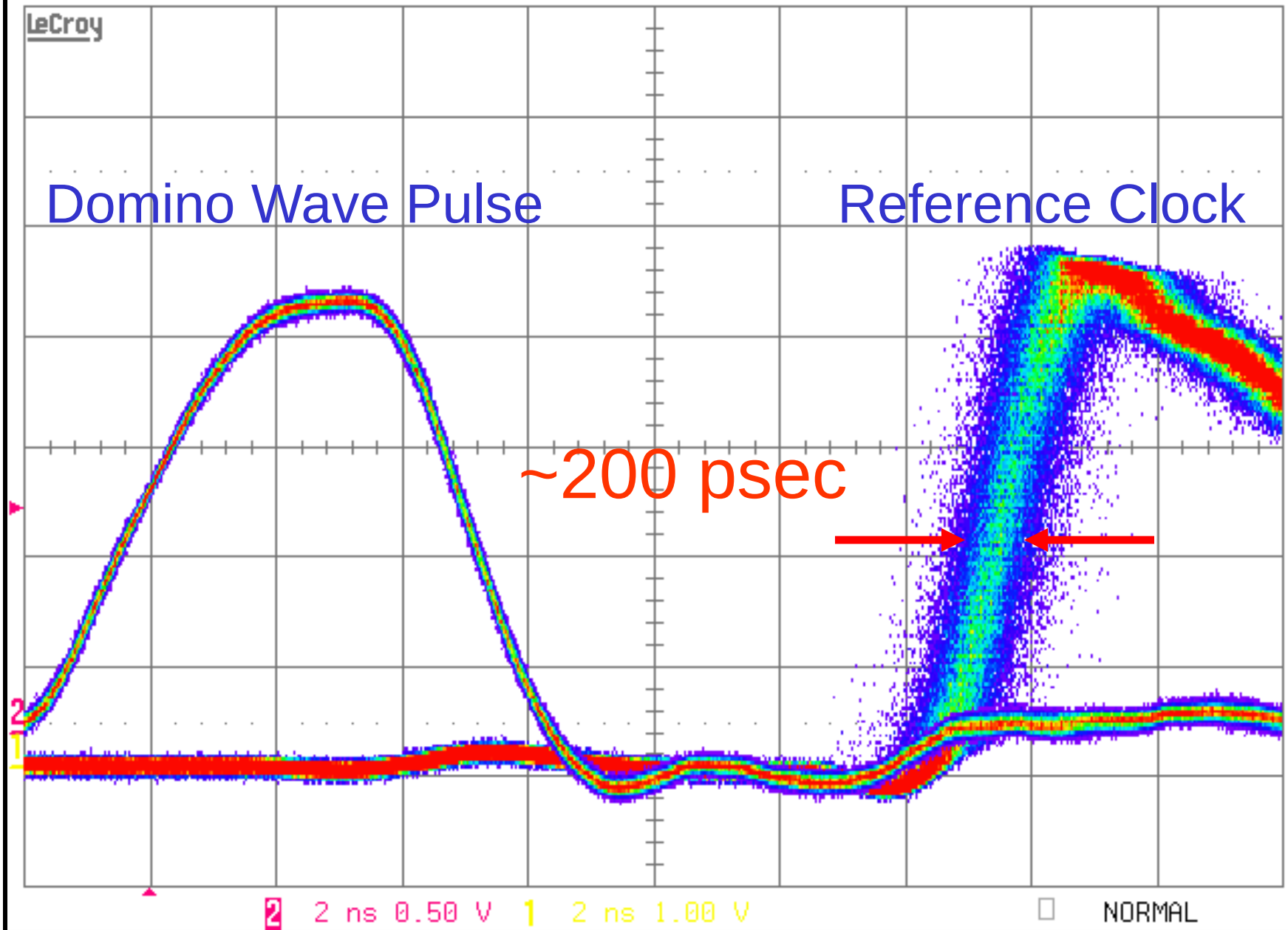
$f_{samp}[GHz]$ vs. $V_{control}[V]$

PLL system and startup optimization



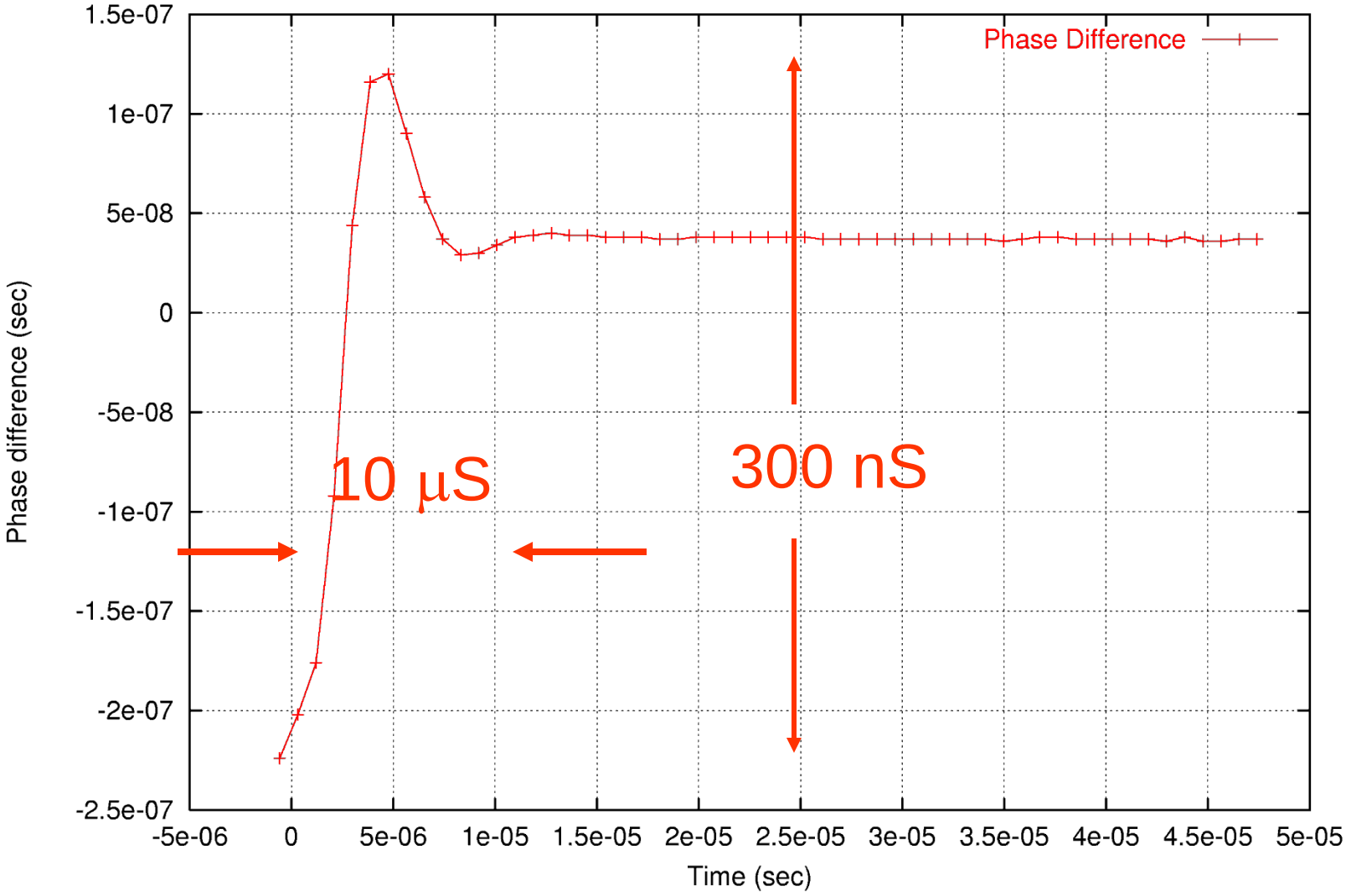
Ideas: starting the Domino Wave in phase with the reference clock (SWITCH) and with the correct speed (ADC-DAC)

PLL: Domino Wave jitter



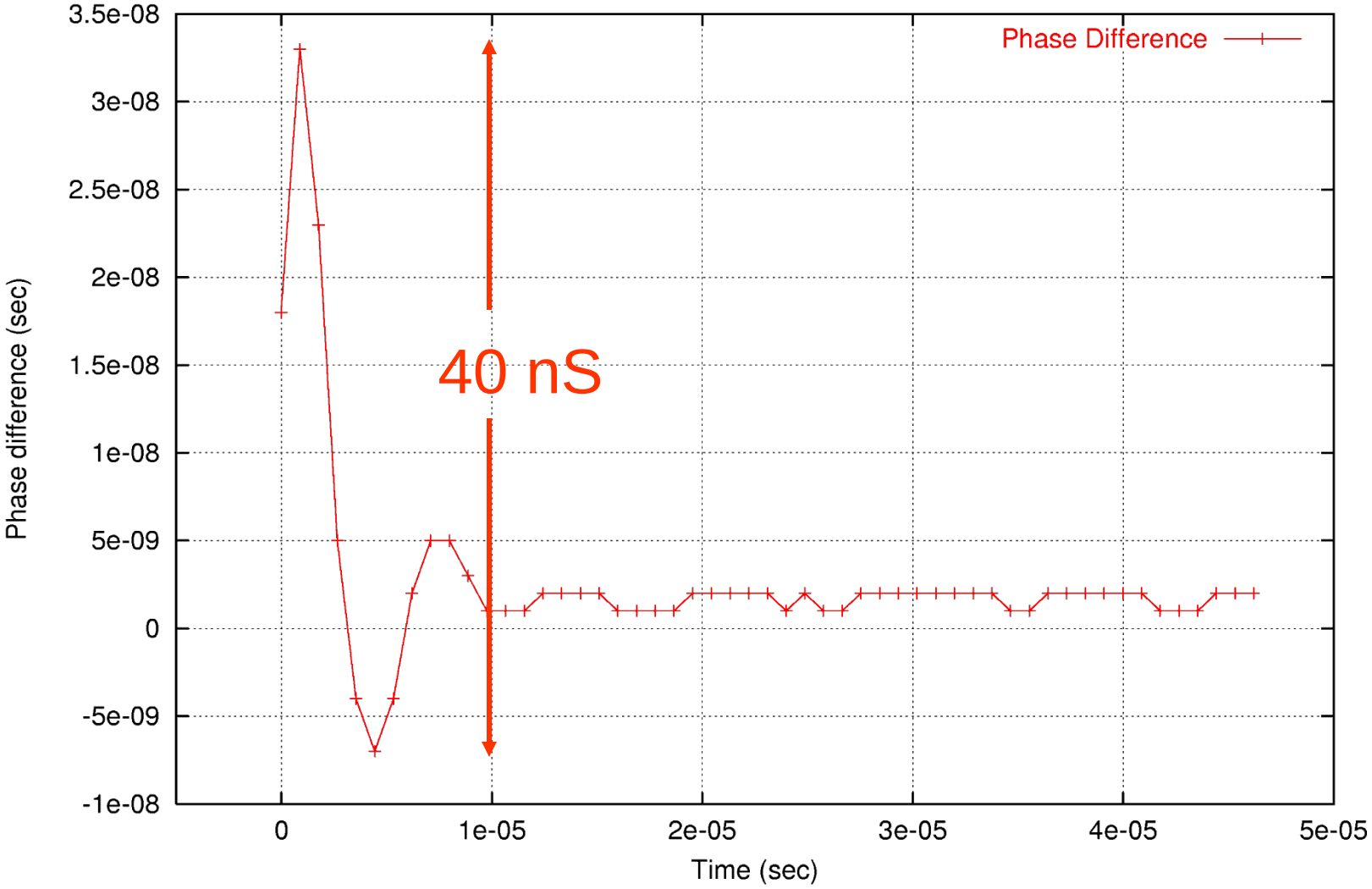
Starting and locking the domino Wave:

Asynchronous starting sequence

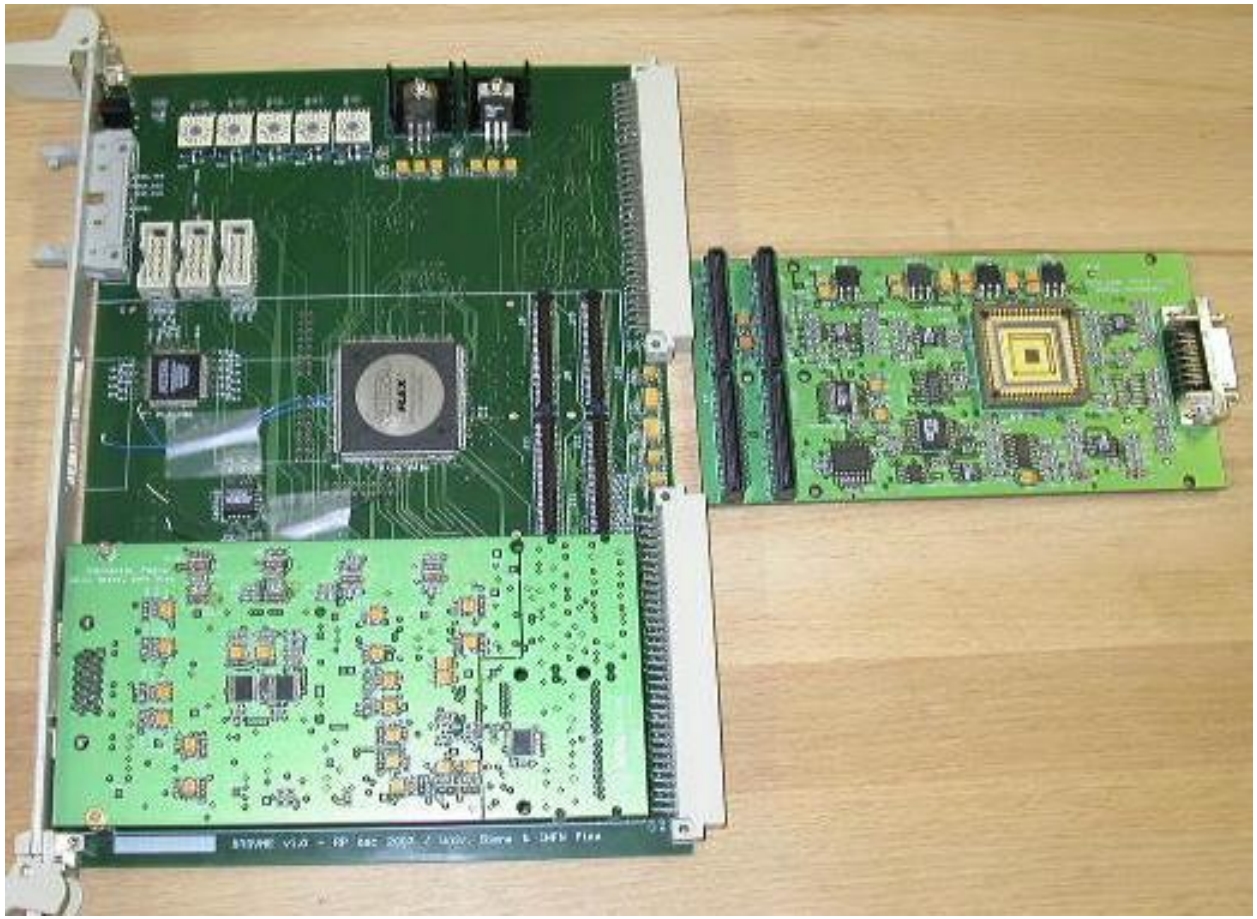


Starting and locking the domino Wave:

Optimized starting sequence



VME Mezzanine carrier board



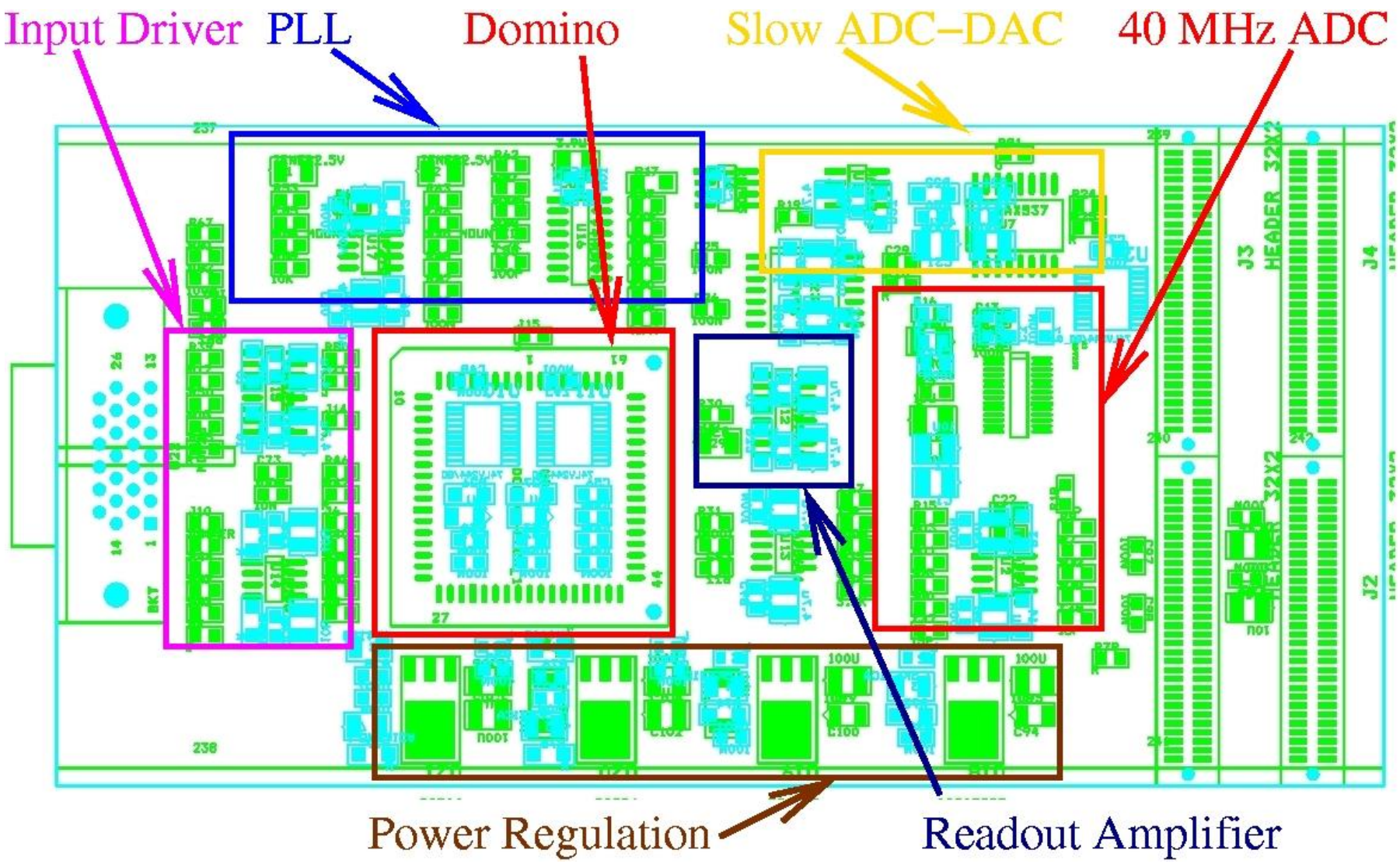
DRS 1st Prototype

- Analog signals only in the mezzanine
- Based on Altera FPGA
- On Board Data reduction
- Big Event Fifo Buffer
- On Board Trigger TDC
- Locking to external clock

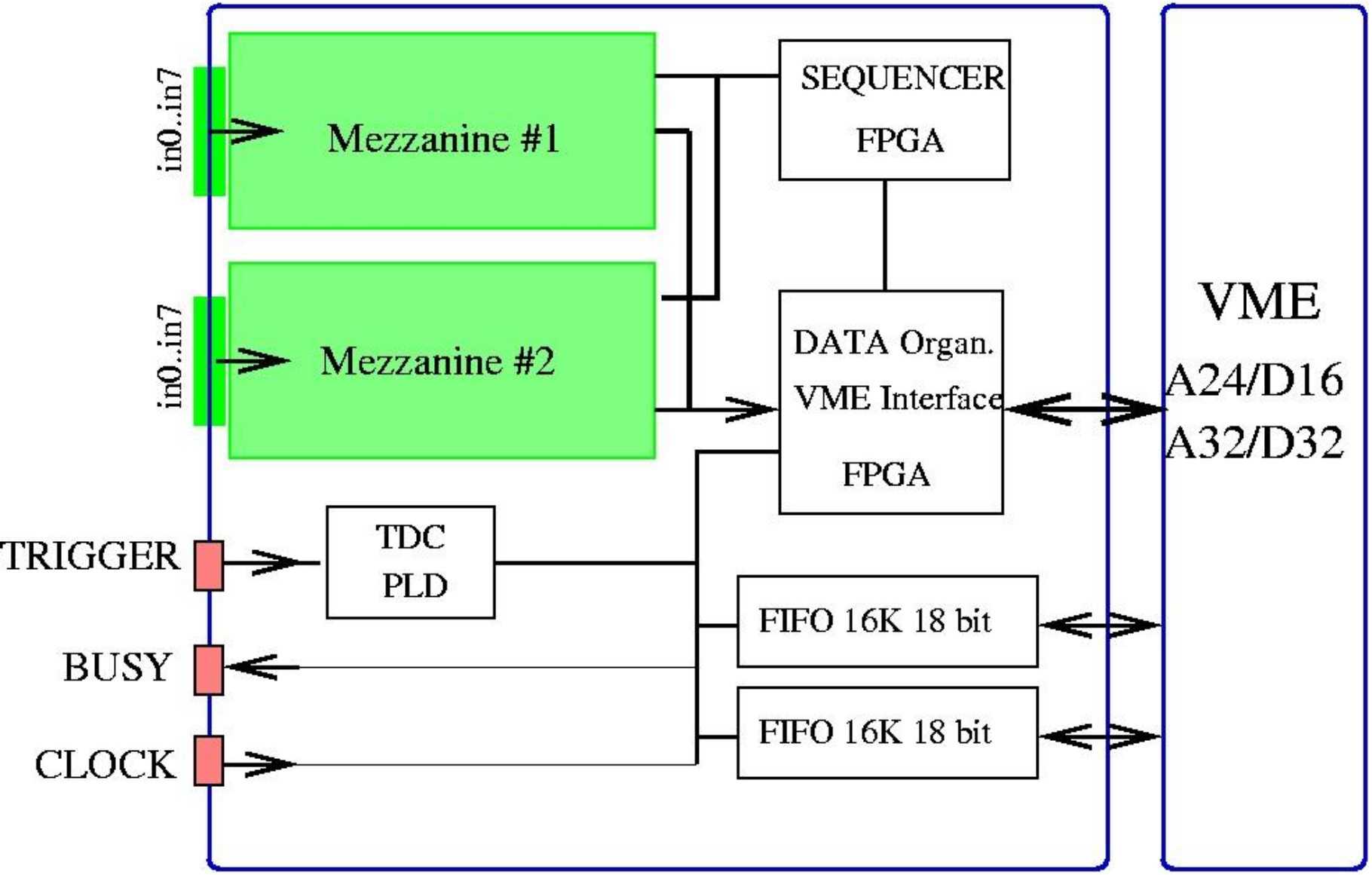
Designed to accept DRS2 and following Domino Chips.

Follows the Common Mezzanine Card Family Standard

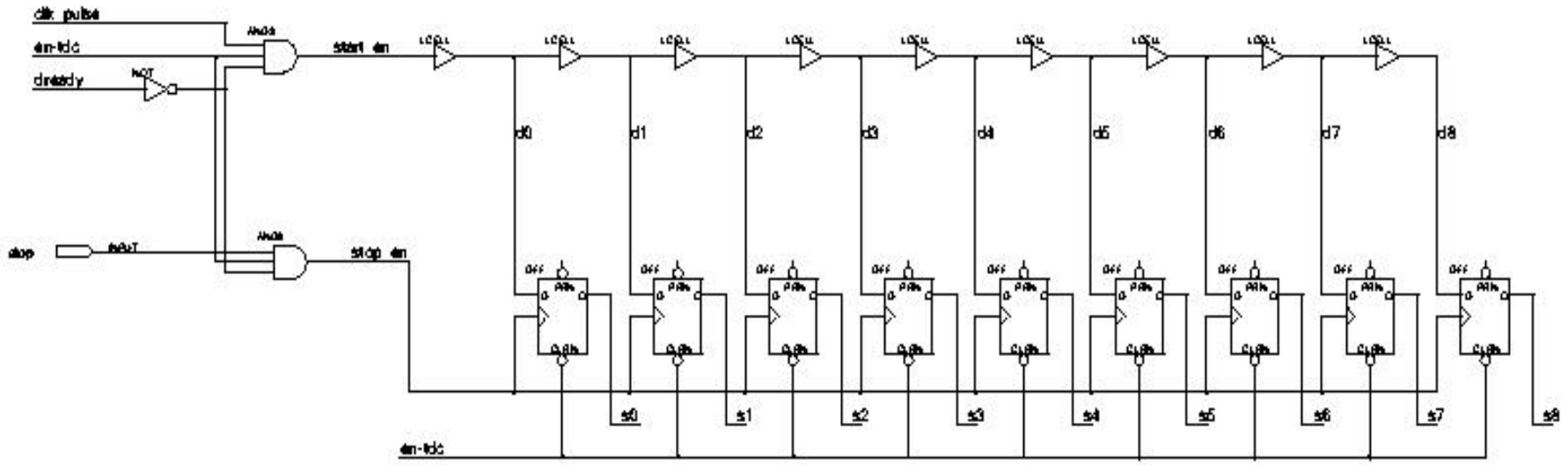
Domino1 Mezzanine Board



VME DRS BOARD



The TDC



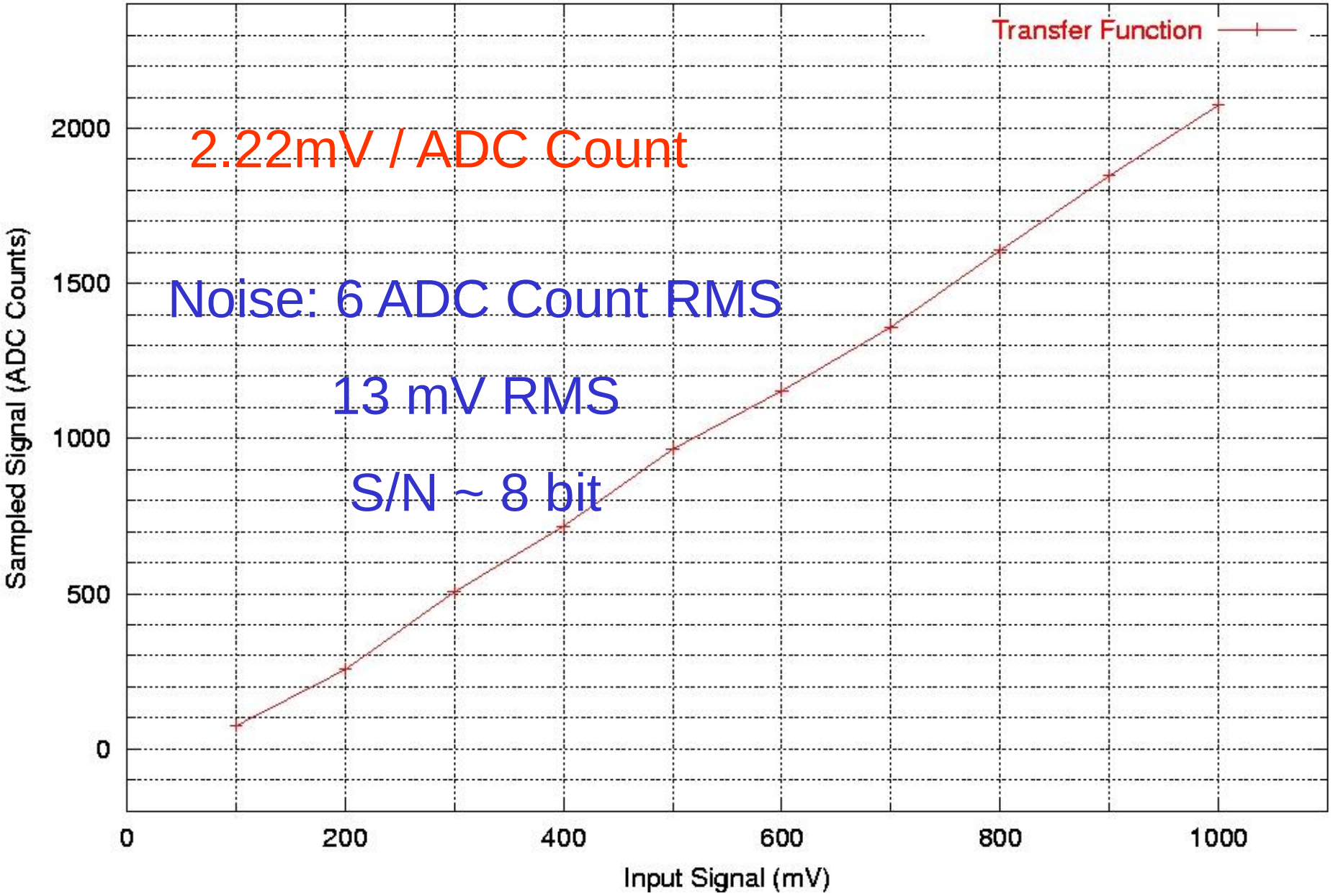
Implemented in a EPM7064BTC100-3

The trigger signal memorize the position of a propagating pulse started by the 40 MHz clock.

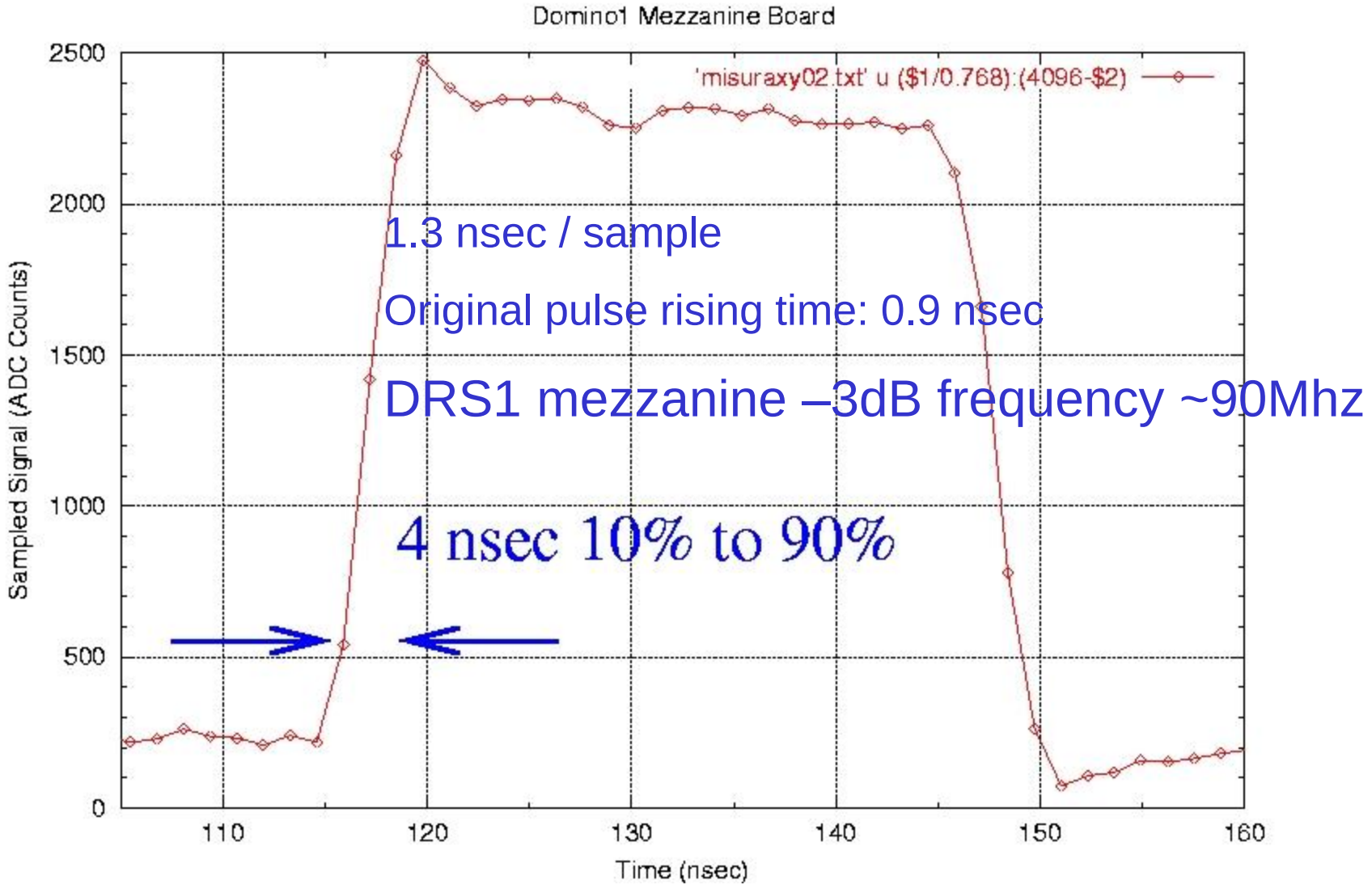
Measure the time between trigger and domino wave synchronisation pulse.

3 nsec Expected Resolution

Domino1 Mezzanine Transfer Function

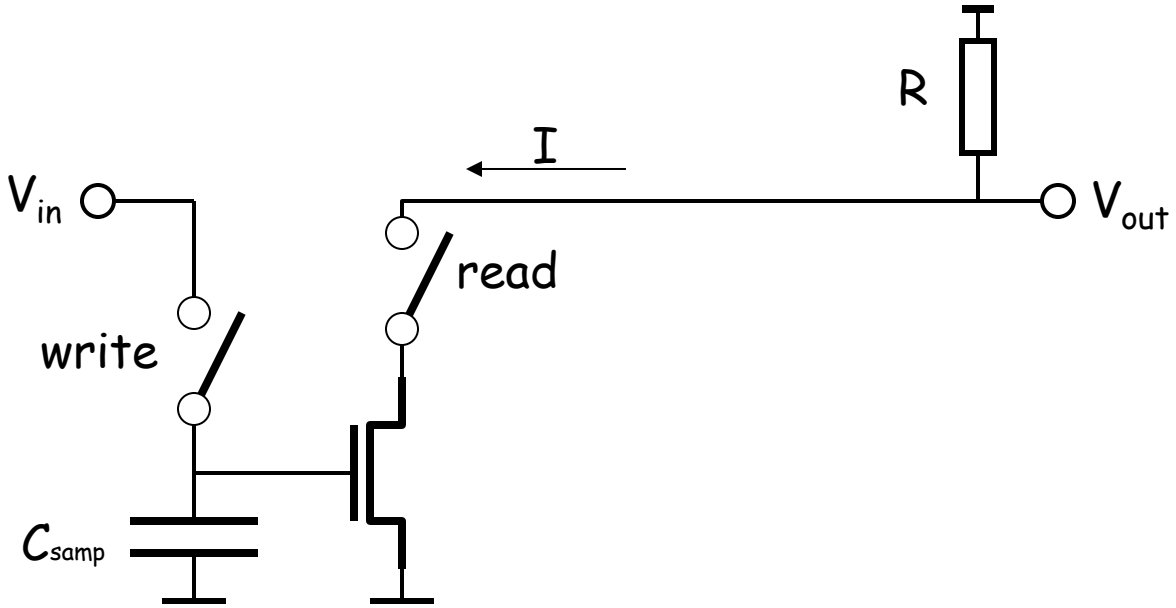


A signal sampled with the DRS1 Mezzanine

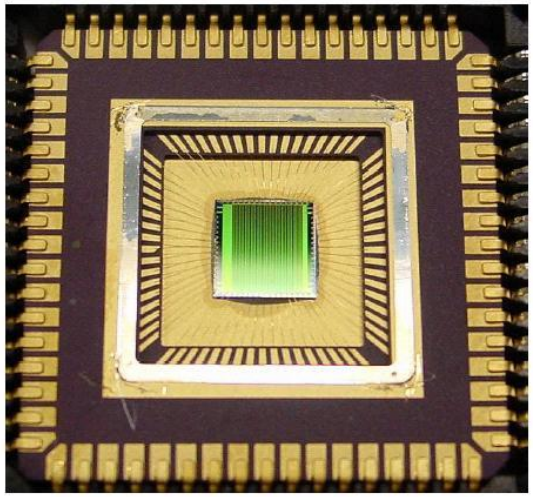


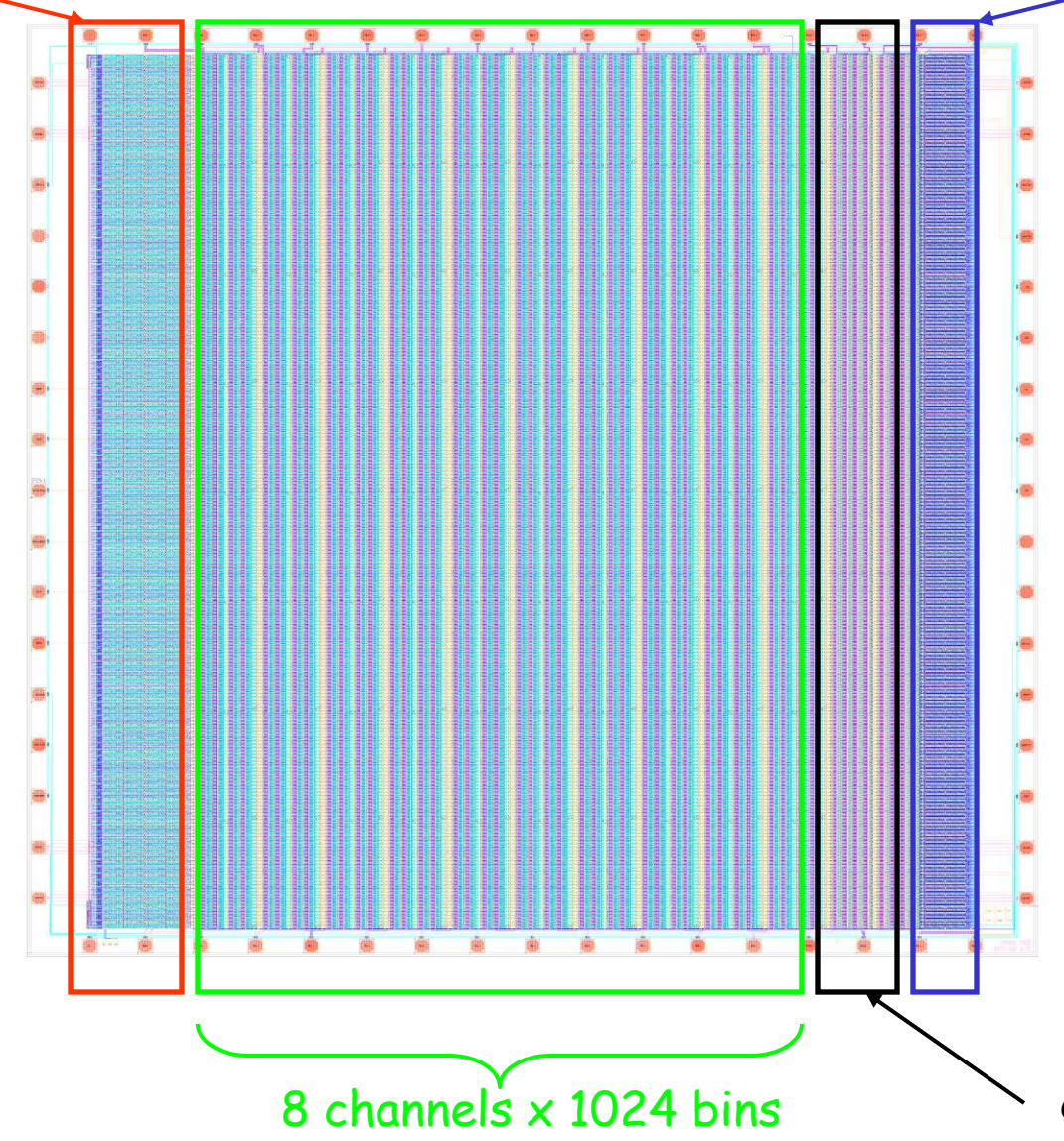
DRS Redesigned

- Reduced bus-bulk capacitance by 6x
- Reduced bus-bus capacitance
- Used current-mode readout

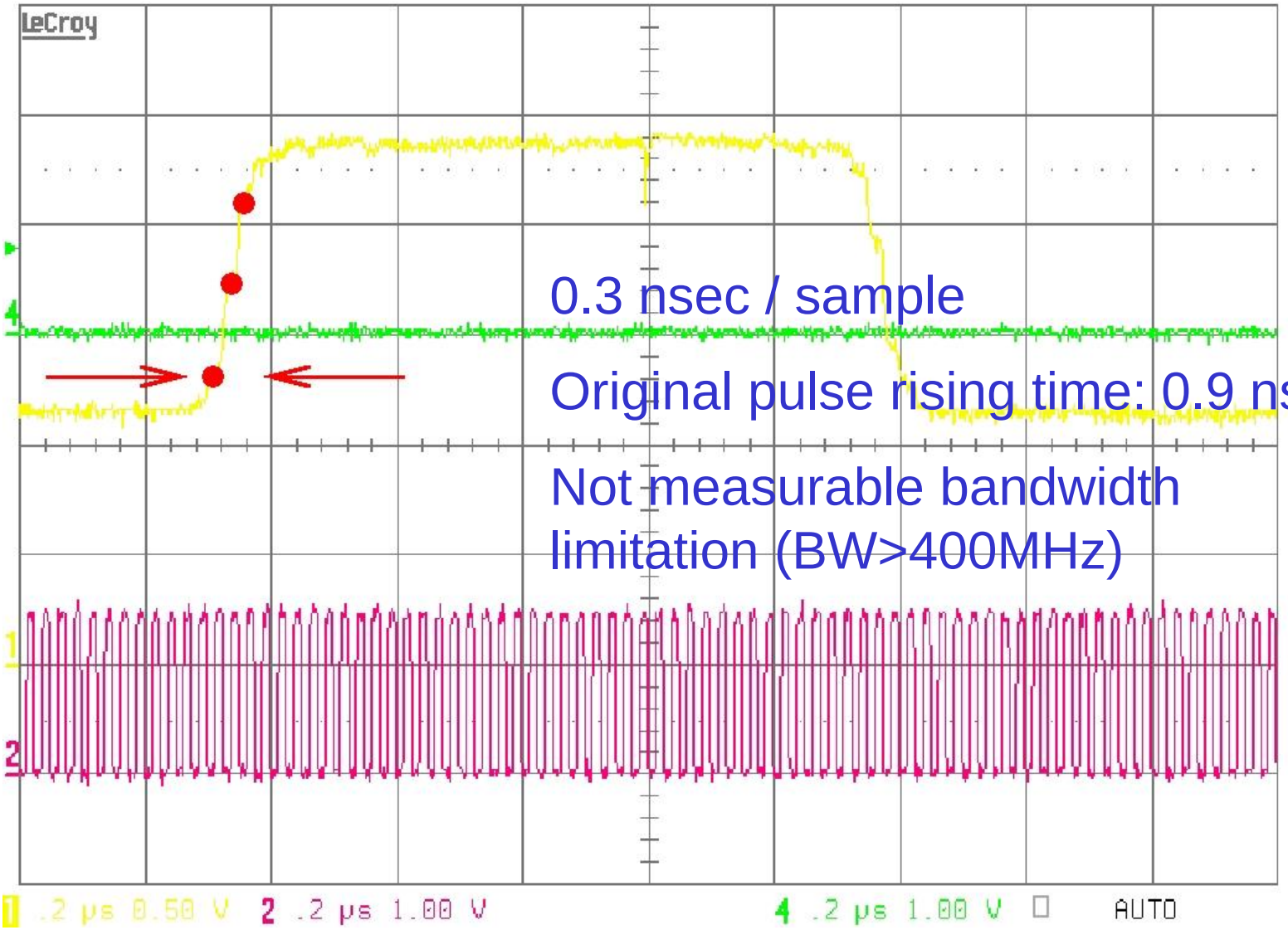


DRS2 Chip layout

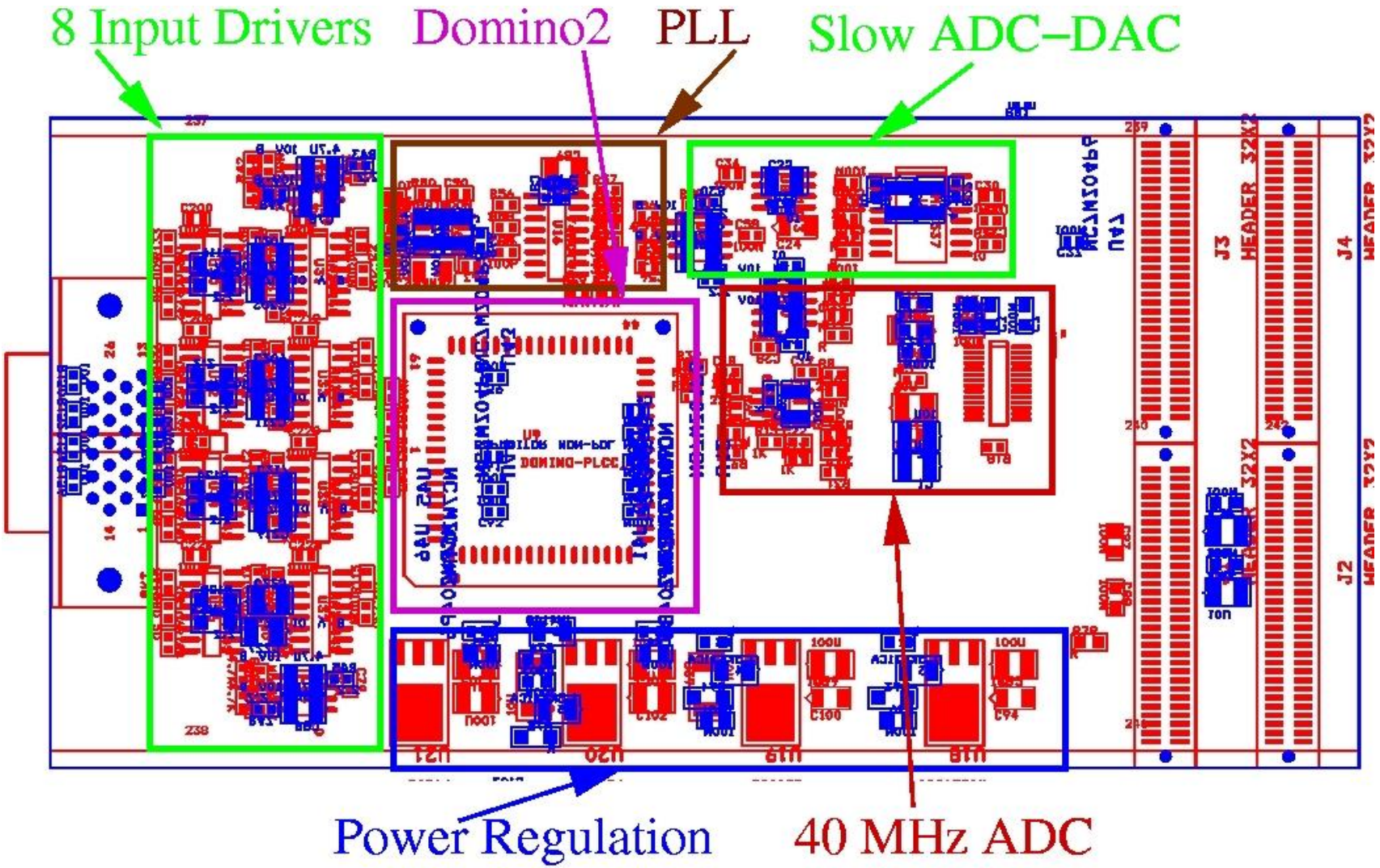




A signal sampled with the DRS2

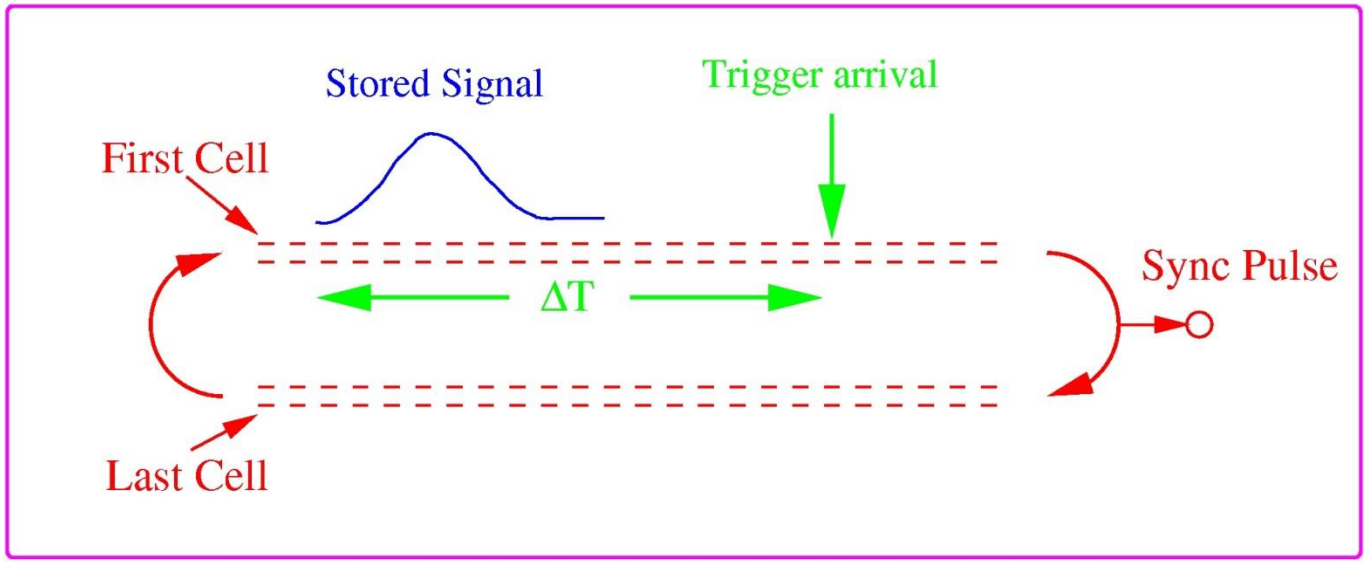


Domino2 and 3 Mezzanine

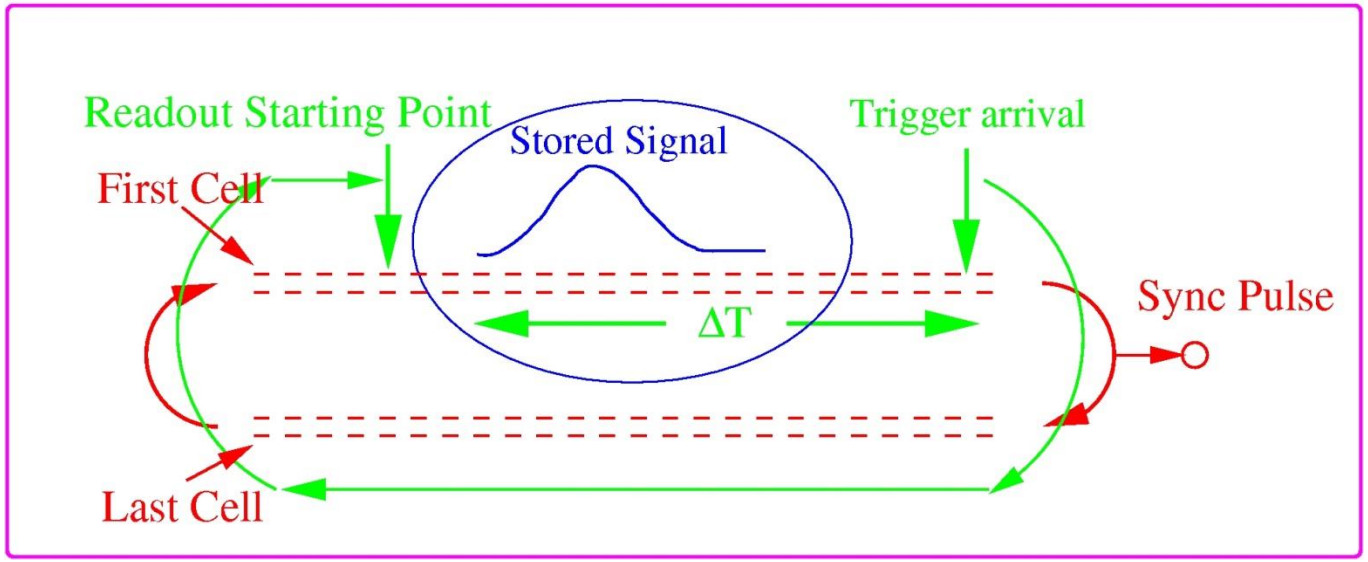


We are designing now this board

Speeding up the readout



Domino1 and 2: readout starts from the first cell; to catch the signal the whole analog memory ring must be read out.



Next Domino: readout will start from the point set by the arrival time of an external signal (delayed trigger); only the interesting part is read out.

Basic Parameters

	DRS1	DRS2
•Number of channels/mezzanine	1	10
•Number of cells/channel	768	1024
•Maximum sampling Speed (GHZ)	2.5	4.5
•Minimum sampling Speed (GHZ)	0.7	1.5
•Readout Speed (MHZ)	40	40
•Readout dead time (μsec)	40	256 (10 chn.)
•Signal to noise ratio (bit)	--	11 (estimated)
•Power consumption (Chip)(mW)	25	50

Conclusions

We propose the DRS-VME board for new DAQ of the Magic experiment.

Two chips with 16 signal channels will be housed on a VME board.

The VME board hosts also a FPGA for data processing, a FIFO, four test channels, and TDC.

A last prototype chip, designed by Stefan Ritt, is planned for fall 2004 implementing an improved 10 times faster readout scheme.