CARLOSrx rel 12.0 reference manual

Samuele Antinori, Filippo Costa, Davide Falchieri

Department of Physics and INFN Bologna

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Configuration file format

	number of words to be read from the RAM			
CARLOSrx	*10xxxxxx*	11-PP-TP-active	anode length	load trigger
CARLOS	*11xxxxxx*	*address*	*address*	*address*
	TH ch1	TH ch0	TL ch1	TL ch0
	stop if error	enable 2D	anode length ch1	anode length ch0
	FF	FF	FF	read back
AMBRA ch0 x4	*0000xx10*	*address*	*address*	*address*
	tx address	read counter	write counter	SOP delay
	FF	FF	baseline present	read back
	baseline 3	*baseline 2*	*baseline 1*	*baseline 0*
	…	…	…	…
	baseline 63	*baseline 62*	*baseline 61*	*baseline 60*
PASCAL ch0 x4	*0000xx00*	*address*	*address*	*address*
	calibration DAC		VREF control DAC	
	ADC full	AM full	gain control	sel cal channels
	FF	FF	FF	read back
AMBRA ch1 x4	*0010xx10*	*address*	*address*	*address*
	tx address	read counter	write counter	SOP delay
	FF	FF	baseline present	read back
	baseline 3	*baseline 2*	*baseline 1*	*baseline 0*
	…	…	…	…
	baseline 63	*baseline 62*	*baseline 61*	*baseline 60*
PASCAL ch1 x4	*0010xx00*	*address*	*address*	*address*
	calibration DAC		VREF control DAC	
	ADC full	AM full	gain control	sel cal channels
	FF	FF	FF	read back

Table 1: Configuration file format

Notes:

- For stopiferror and enable 2D the following encoding has been used:
  - 0 → 00000000
  - 1 → 01111111
- For ADC full and AM full the following encoding has been chosen:
  - 11111111 → full frequency
  - 00000000 → half frequency
- tx_addr:

    - tx_addr is only written during individual addressing
    - only the 2 LSBs are meaningful for tx_addr.
- The baseline values are 6-bit numbers. Only the 6 LSBs are taken into account.
- 11-PP-TP-active:
    - 11: two fixed bits;
    - PP: prepulse enable bit.
        - When high, an active pre-pulse signal coming from the TTC system is interpreted as a prepulse.
        - When low, an active pre-pulse signal coming from the TTC is discarded.
    - TP: testpulse enable bit.
        - When active, an active pre-pulse signal coming from the TTC system is interpreted as a testpulse.
        - When low, an active pre-pulse signal coming from the TTC is discarded.

      Acceptable configurations for PP and TP bits are:
        - 10: prepulse
        - 01: testpulse
        - 00: no pulse
        - 11: prepulse
    - active modules, four bits:
        - bit 3: when 1, modules 9, 10 and 11 are acquired;
        - bit 2: when 1, modules 6, 7 and 8 are acquired;
        - bit 1: when 1, modules 3, 4 and 5 are acquired;
        - bit 0: when 1, modules 0, 1 and 2 are acquired;

Front-end chips configuration files

PASCAL.config:

READ_REG	Y
VALUE VREF CONTROL DAC	75
VALUE CALIBR DAC	511
VALUE SELECT CALIBRATION	21
VALUE GAIN CONTROL	3
SET AM FULL	Y
SET AM HALF	N
SET ADC FULL	Y
SET ADC HALF	N
READ AM ADC FREQ	Y

AMBRA.config:

READ_REG	Y
VALUE SOP DELAY	160
VALUE WCNT STOP	255
VALUE RCNT STOP	255
WRITE BASELINE	N

CARLOS.config:

AL RIGHT	255
AL LEFT	255
TL RIGHT	0
TL LEFT	0
TH RIGHT	0
TH LEFT	0
ENABLE 2D	Y
READ REG	Y
STOP IF ERROR	0

CARLOSRX.config:

VALUE AL CARLOSRX	255
VALUE TRIGGER	209