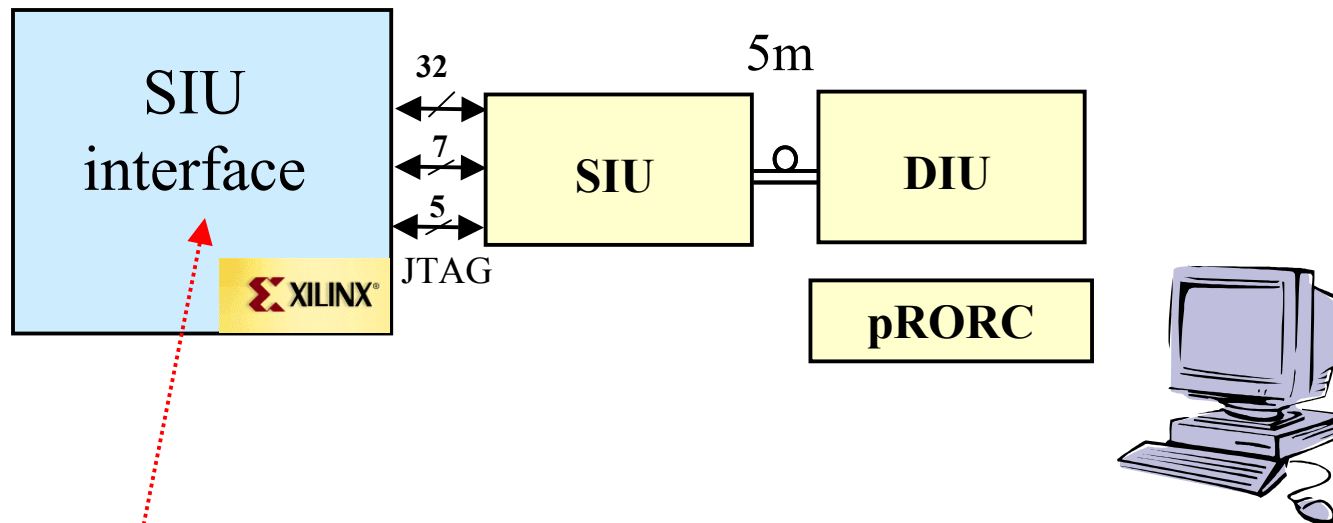


Status of the integration of the ITS Drift chain with the DDL

INFN Bologna

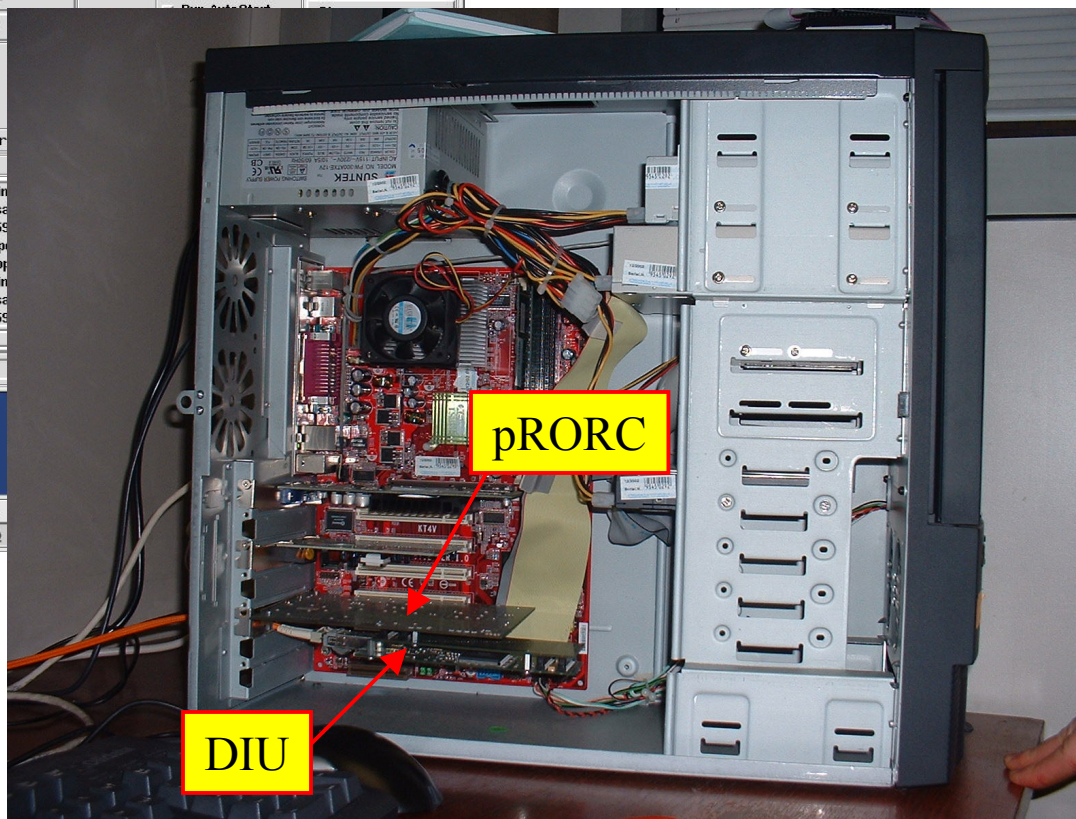
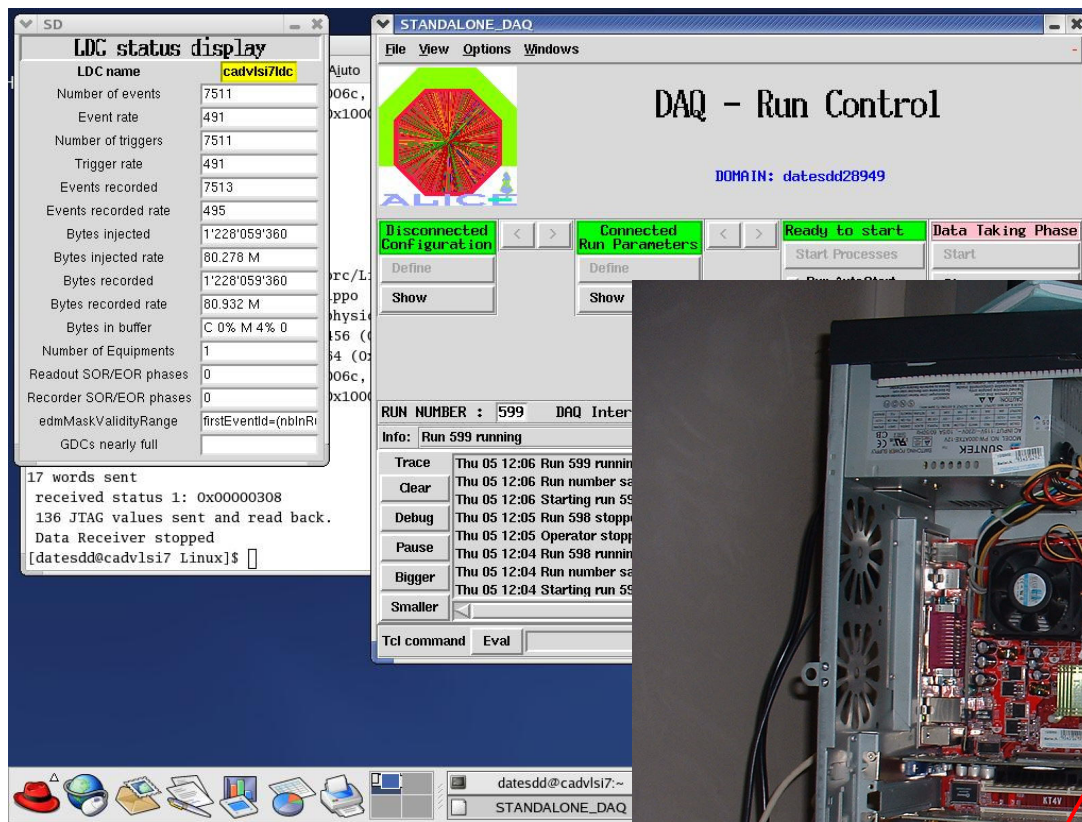
Readout chain implementation in Lab

- CERN DDL installation (SIU + optical fibre + DIU + pRORC + DATE v4.6)



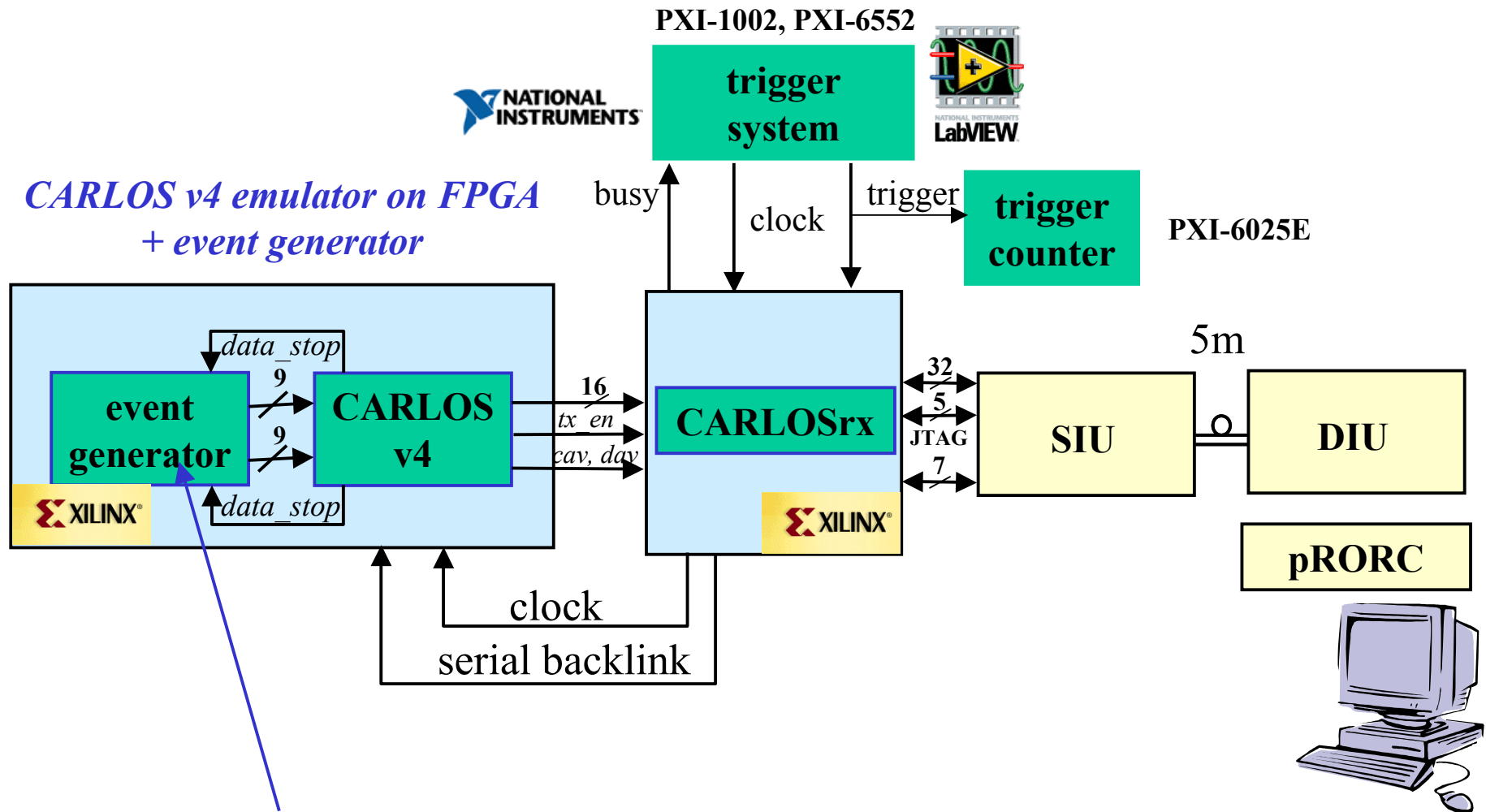
FPGA (Virtex XC2V1000) implementation of the SIU interface for a preliminary test of the DDL

DATE 4.6 & DIU - pRORC



Readout chain implemented in Lab

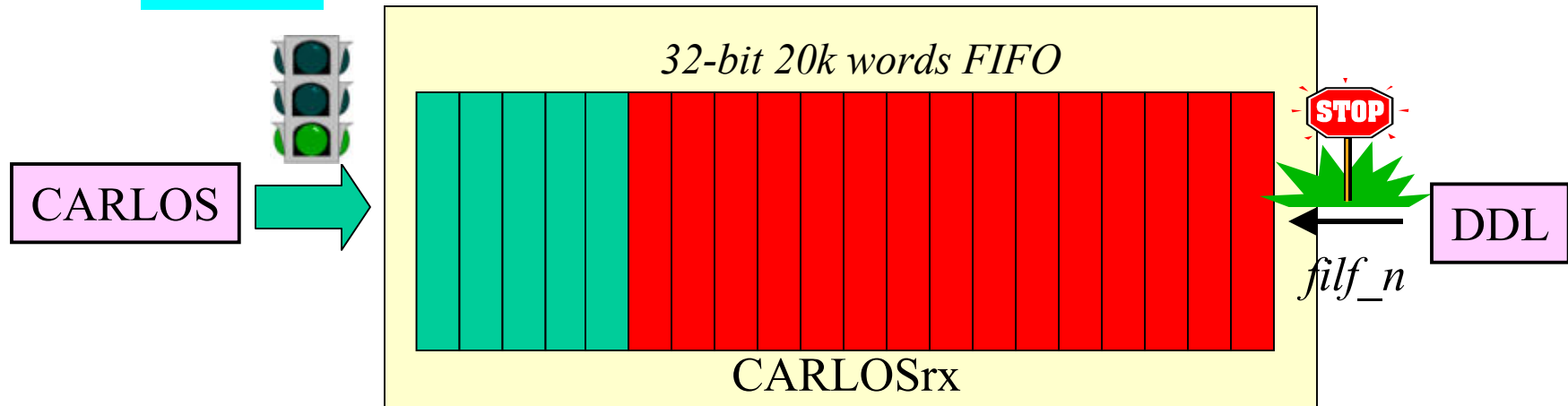
(before receiving CARLOS v4 ASIC)



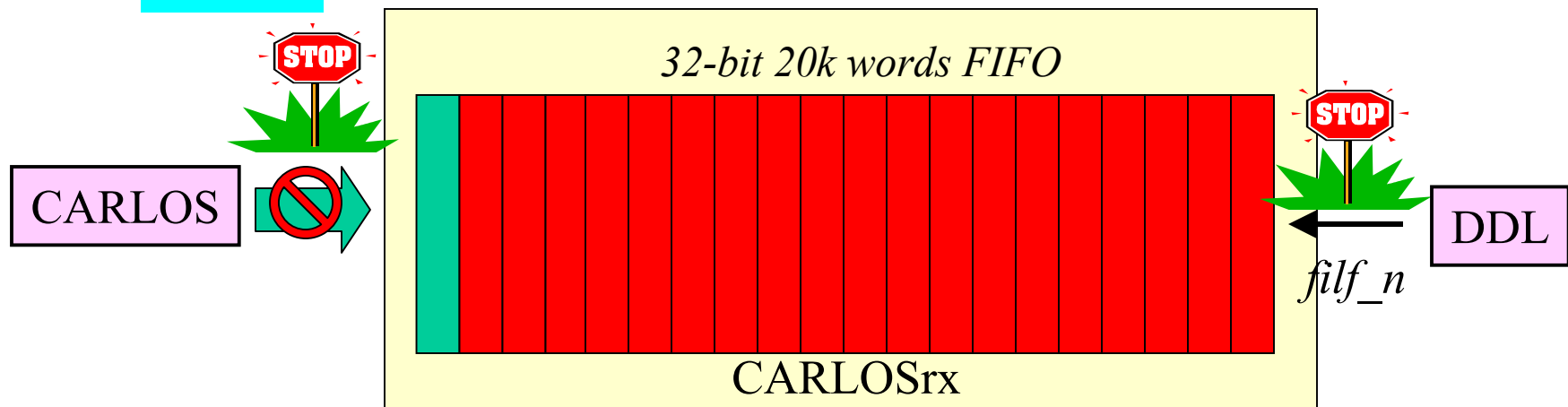
The **event generator** block (on the same FPGA as CARLOS) sends to CARLOS the same event each time it receives a trigger

Flow control implemented on CARLOSrx

STEP 1



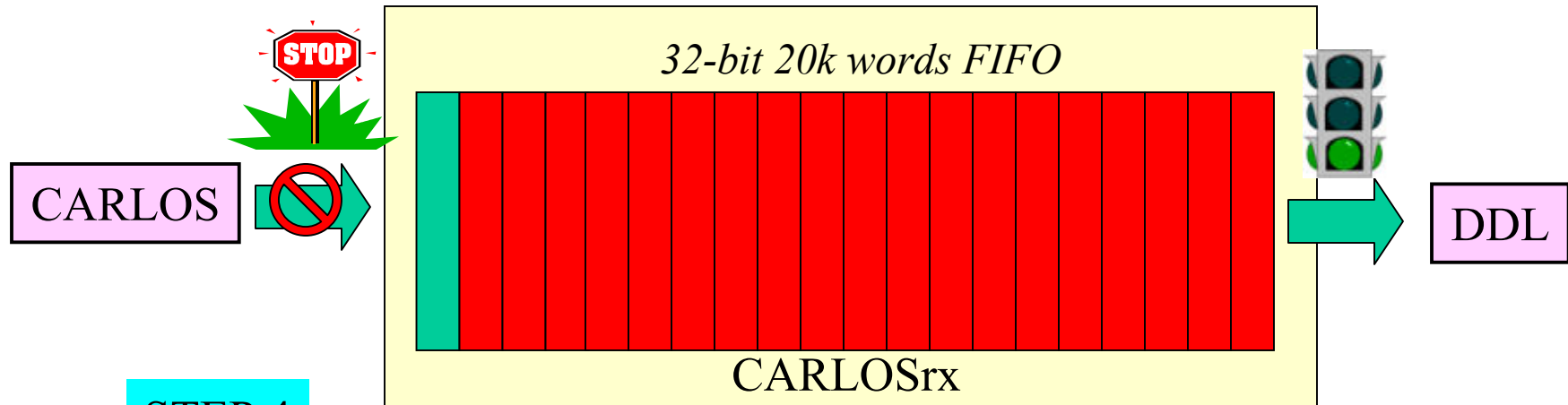
STEP 2



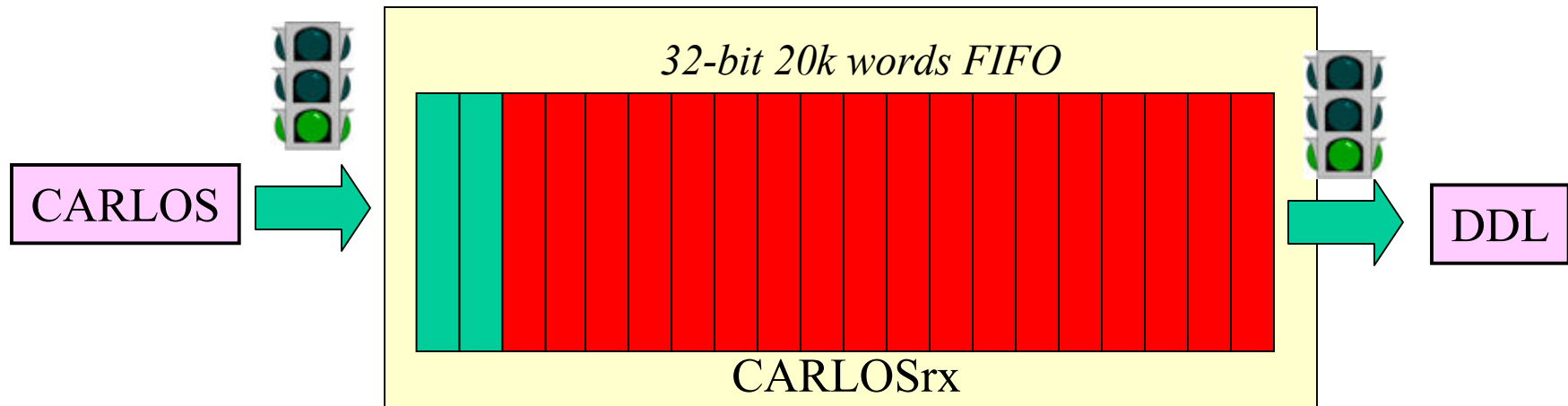
CARLOSrx asserts the back-pressure towards CARLOS

Flow control implemented on CARLOSrx

STEP 3



STEP 4



CARLOSrx de-asserts the back-pressure towards CARLOS

Snapshot taken during data acquisition



Number of trigger sent

device
1

port list
0,1

buffer size
10000

scans to read at a time
1000

STOP

Trigger read
49018

Scan Backlog
0

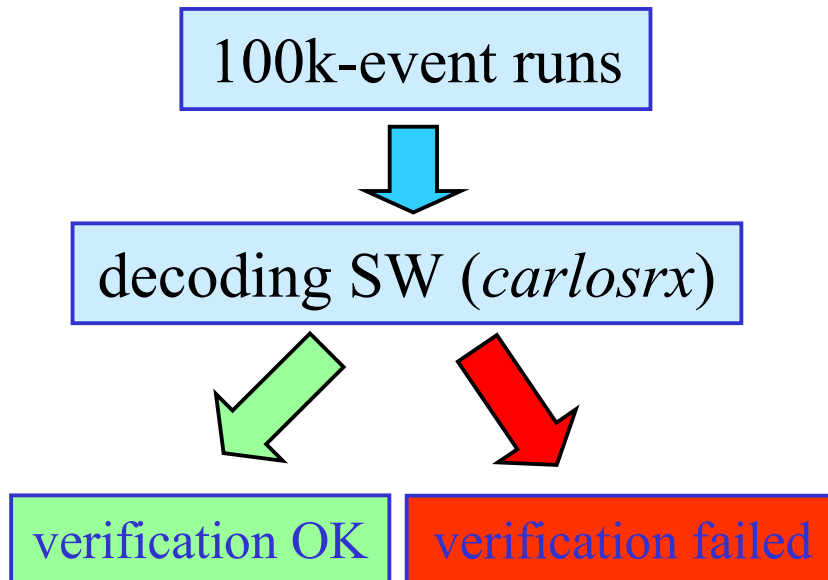
NATIONAL INSTRUMENTS

PXI-6025E

Number of events recorded

LDC status display	
LDC name	cadvlsi7ldc
Number of events	49018
Event rate	0
Number of triggers	49018
Trigger rate	0
Events recorded	49020
Events recorded rate	0
Bytes injected	396'911'224
Bytes injected rate	0
Bytes recorded	396'911'224
Bytes recorded rate	0
Bytes in buffer	C 0% M 1% 0
Number of Equipments	1
Readout SOR/EOR phases	0
Recorder SOR/EOR phases	0
edmMaskValidityRange	firstEventId=(nbInRi
GDCs nearly full	

Verification step



Test features:

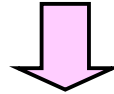
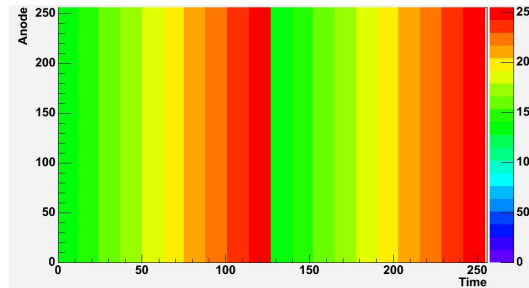
- CARLOS programming via JTAG
- Event sizes: 2.5k, 16k e 64k
- Back-pressure of CARLOSrx over CARLOS
- Programmable trigger frequency

The screenshot shows the SDD (Software Development and Debug) interface. It features a title bar with the text "SDD" and standard window controls. The main area is titled "Options" and contains several input fields and buttons. The input fields are labeled: "Insert RAW number (press return to confirm)", "Insert file number (return)", "Inserisci l'anode length (invio)", "Insert TH 0 (return)", "Insert TH 1 (return)", "Insert TL 0 (return)", and "Insert TL 1 (return)". Each field has a corresponding numeric input box, all of which currently display "0". Below these fields, there is a section for "Compression enable?" with radio buttons for "Yes" and "No", and "No" is selected. Below this is another input field for "Insert limit number (return)" with a value of "0". At the bottom of the interface, there are several buttons: "Print", "Start", "Controlla gli eventi uguali", "IOT", "GRAPH", "MEDIA", and "Exit".

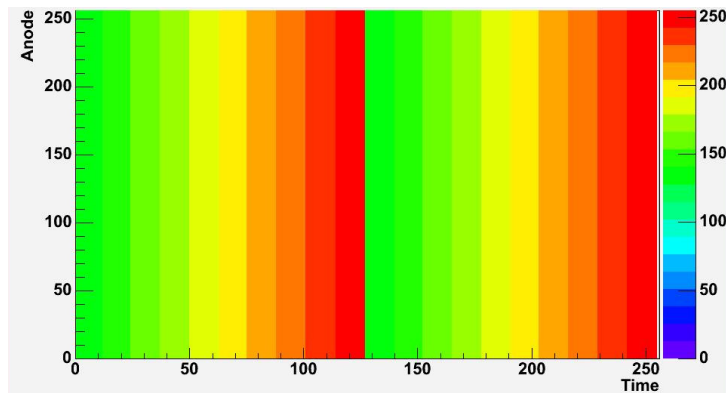
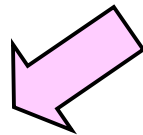
Test of CARLOS v4 (FPGA):

- the interface CARLOS, CARLOSrx, DDL has been successfully tested
- data acquired on PC are correct

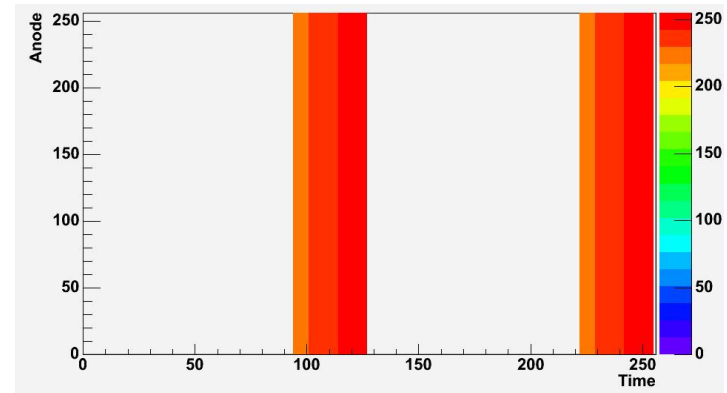
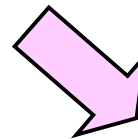
Applying compression to the input pattern



CARLOS – CARLOSrx readout chain

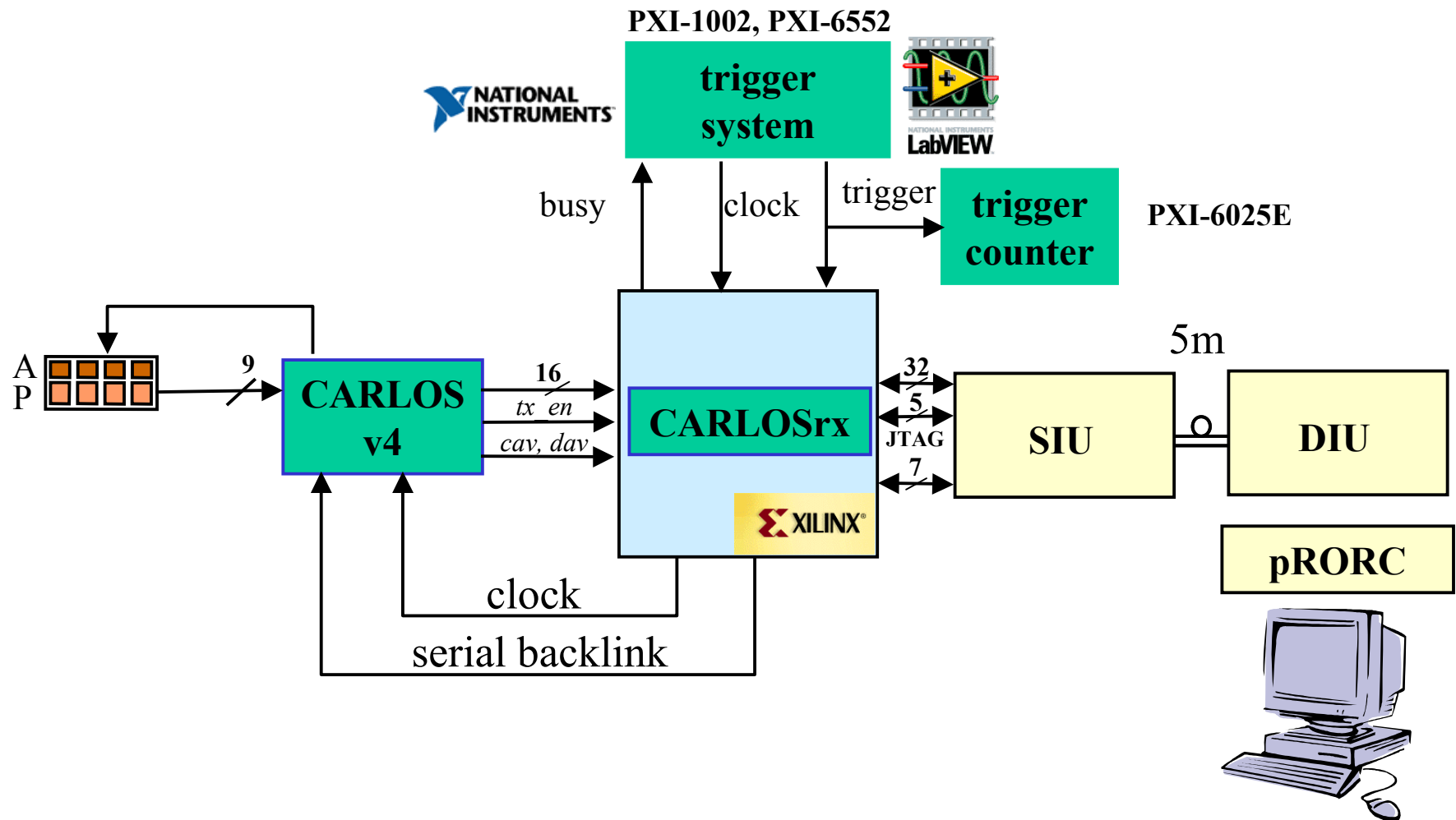


2D compression disabled

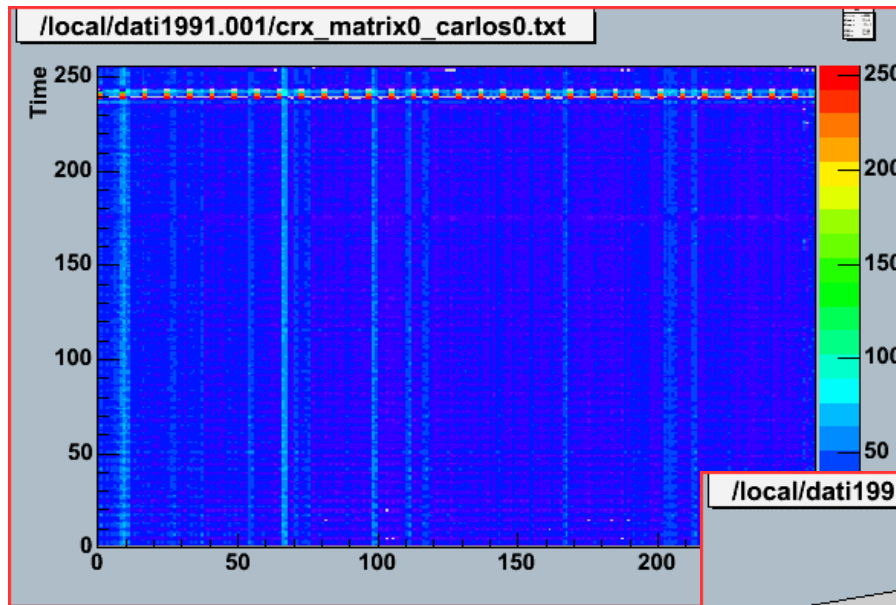


2D compression enabled

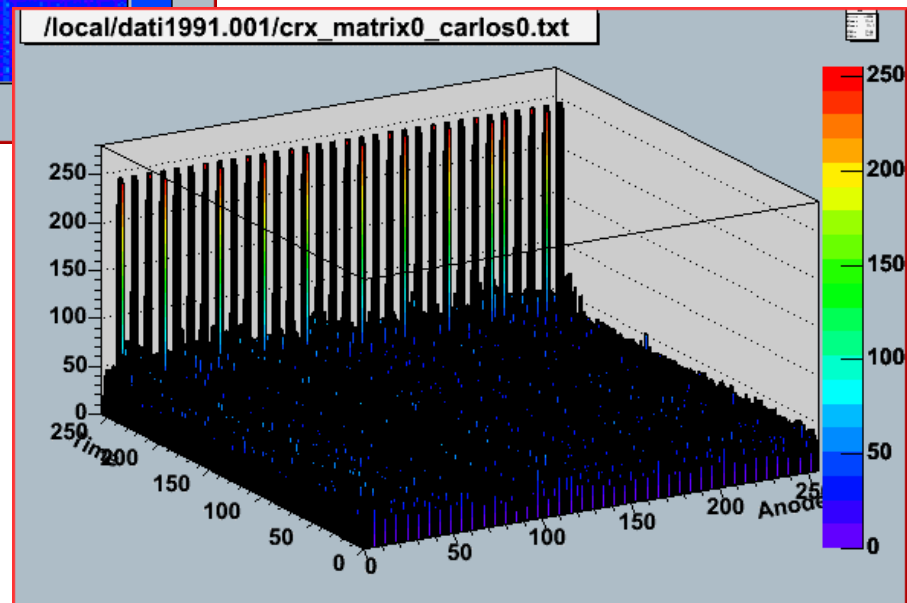
*Readout chain with the **FEE** board and **CARLOS v4 ASIC***



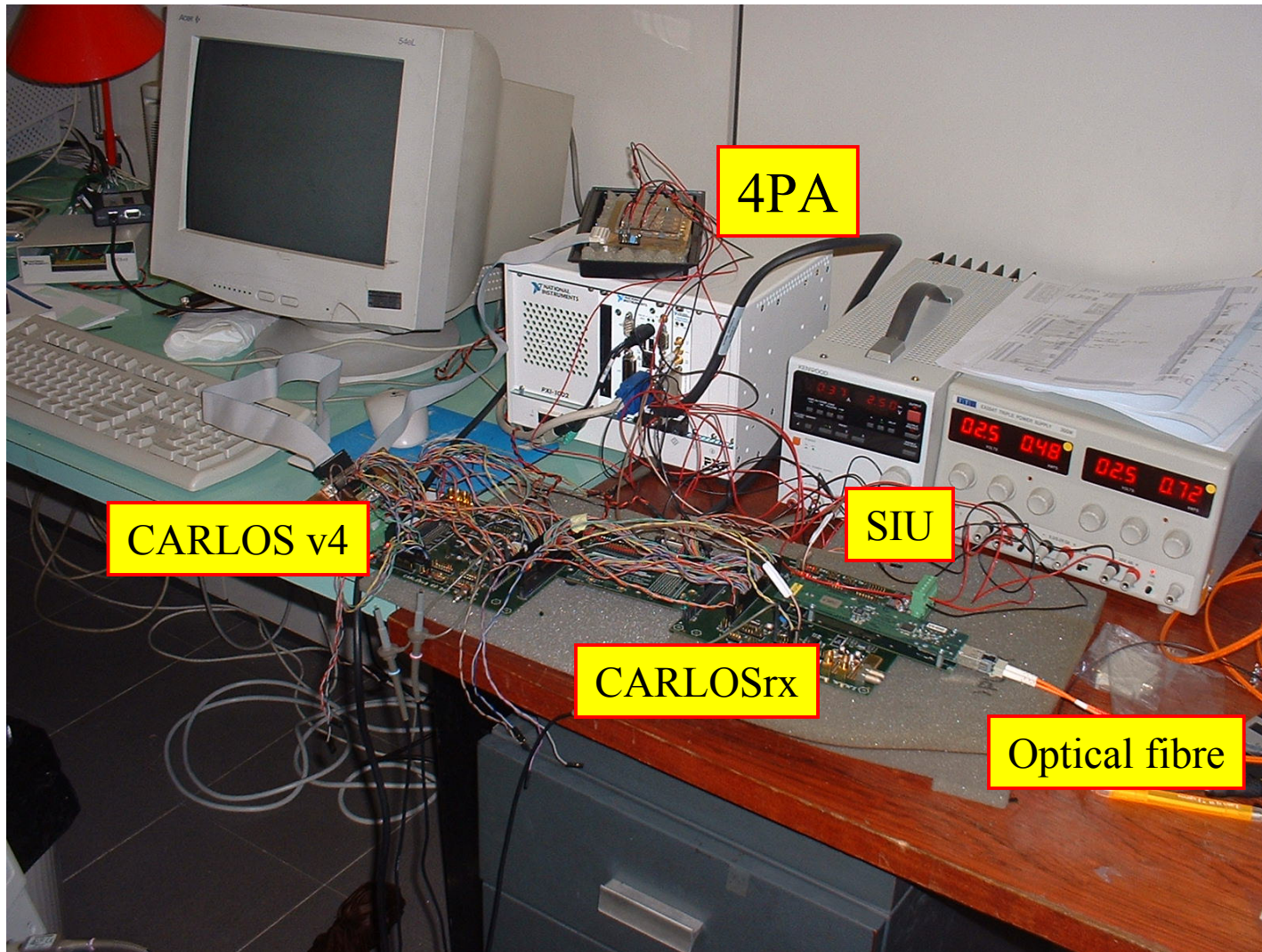
Tests with the FEE board



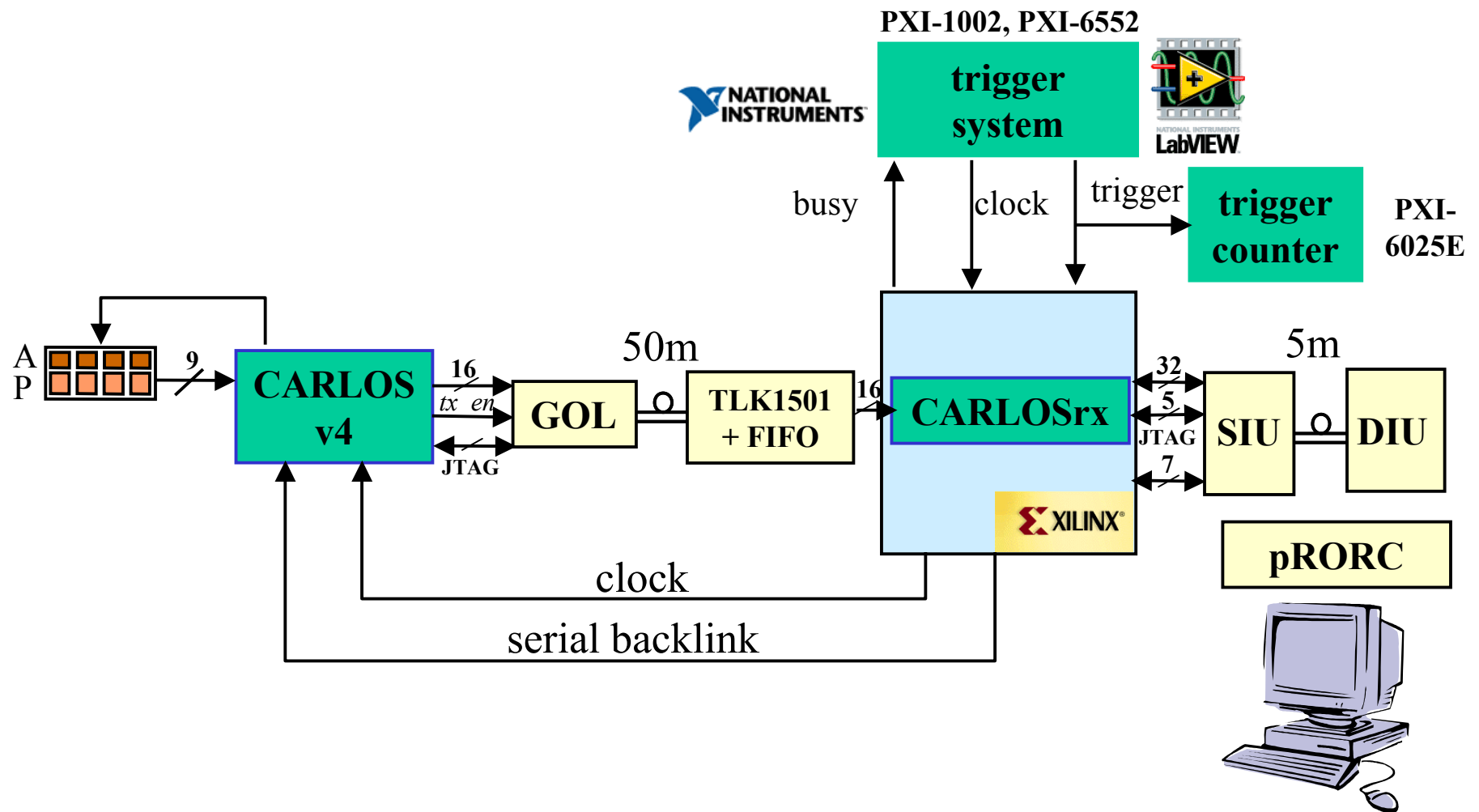
Noise + test pulse with
compression disabled



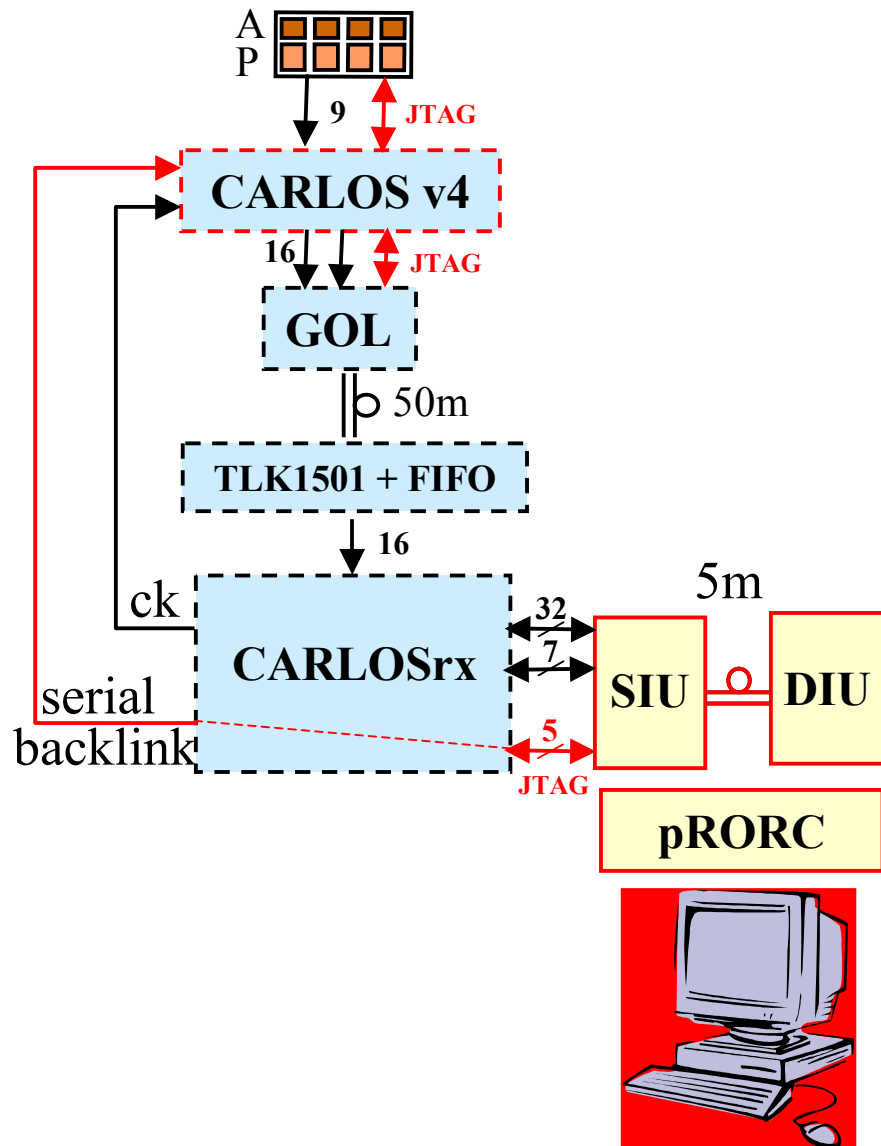
Readout chain (picture)



*Readout chain with **the optical link***



Still to come: JTAG file generator for send_jtag



Jtag file generator

Options

Insert AL left (press return to confirm)

Insert AL right (return)

Insert T1L right (invio)

Insert T1L left 0 (return)

Insert T1H right (return)

Insert T1H left 0 (return)

STOP IF ERROR?

☐ Yes

☐ No

PROG AMBRA?

☐ Yes

☐ No

PROG PASCAL

☐ Yes

☐ No

Read Ambra registers?

☐ Yes

☐ No

Read Carlos registers?

☐ Yes

☐ No

Read Pascal registers?

☐ Yes

☐ No

Compression enable?

☐ Yes

☐ No

Calculate parity?

☐ Yes

☐ No

Print

JTAG

Exit

Conclusions

- The DDL, pRORC and DATE allowed us to acquire a very huge amount of data (very soon we had to buy a new 250 GB disk !) and to study very carefully the behaviour of the readout chain.
- We plan to use the DDL, pRORC and DATE acquisition system for the forthcoming tests.
- Attempts to install and use MOOD were not successful.