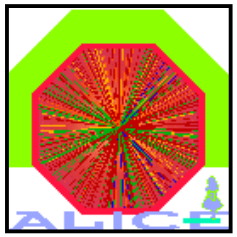
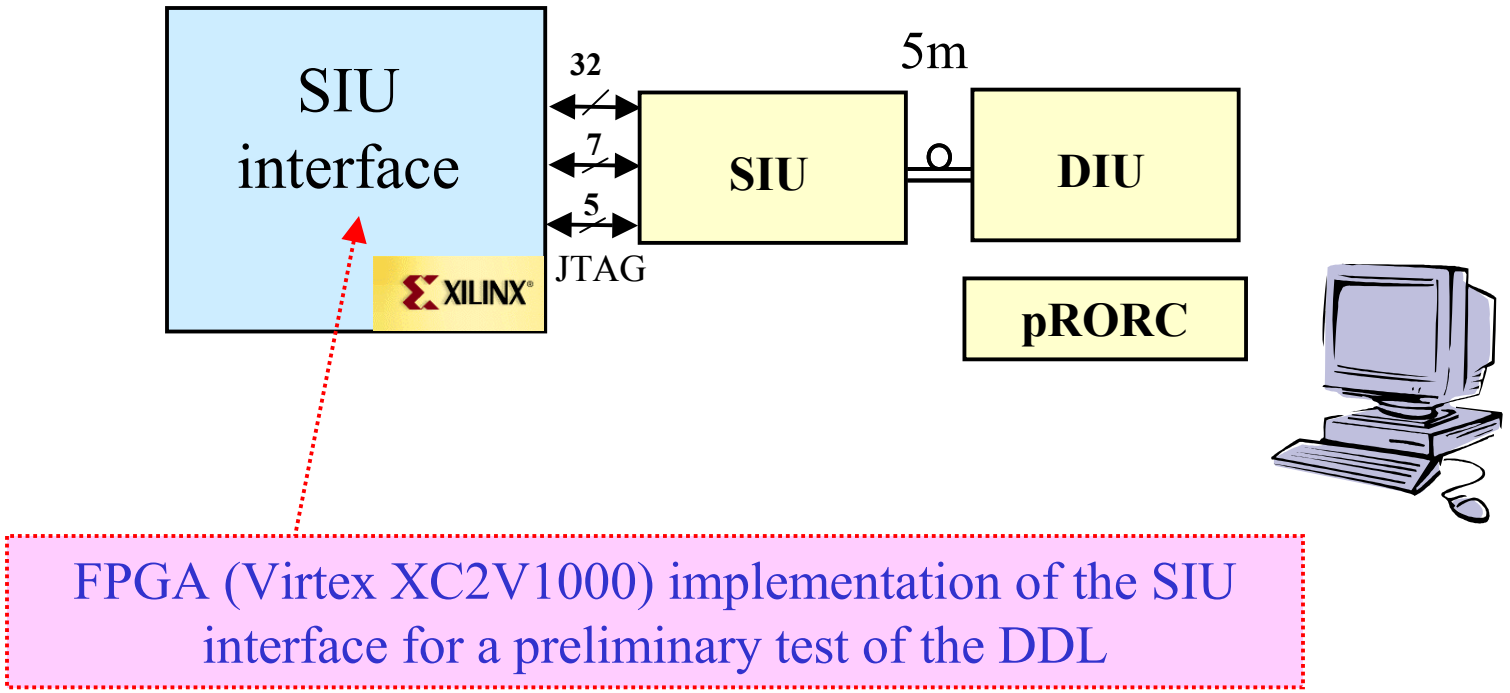


Status of the integration of the ITS Drift chain with the DDL

INFN Bologna

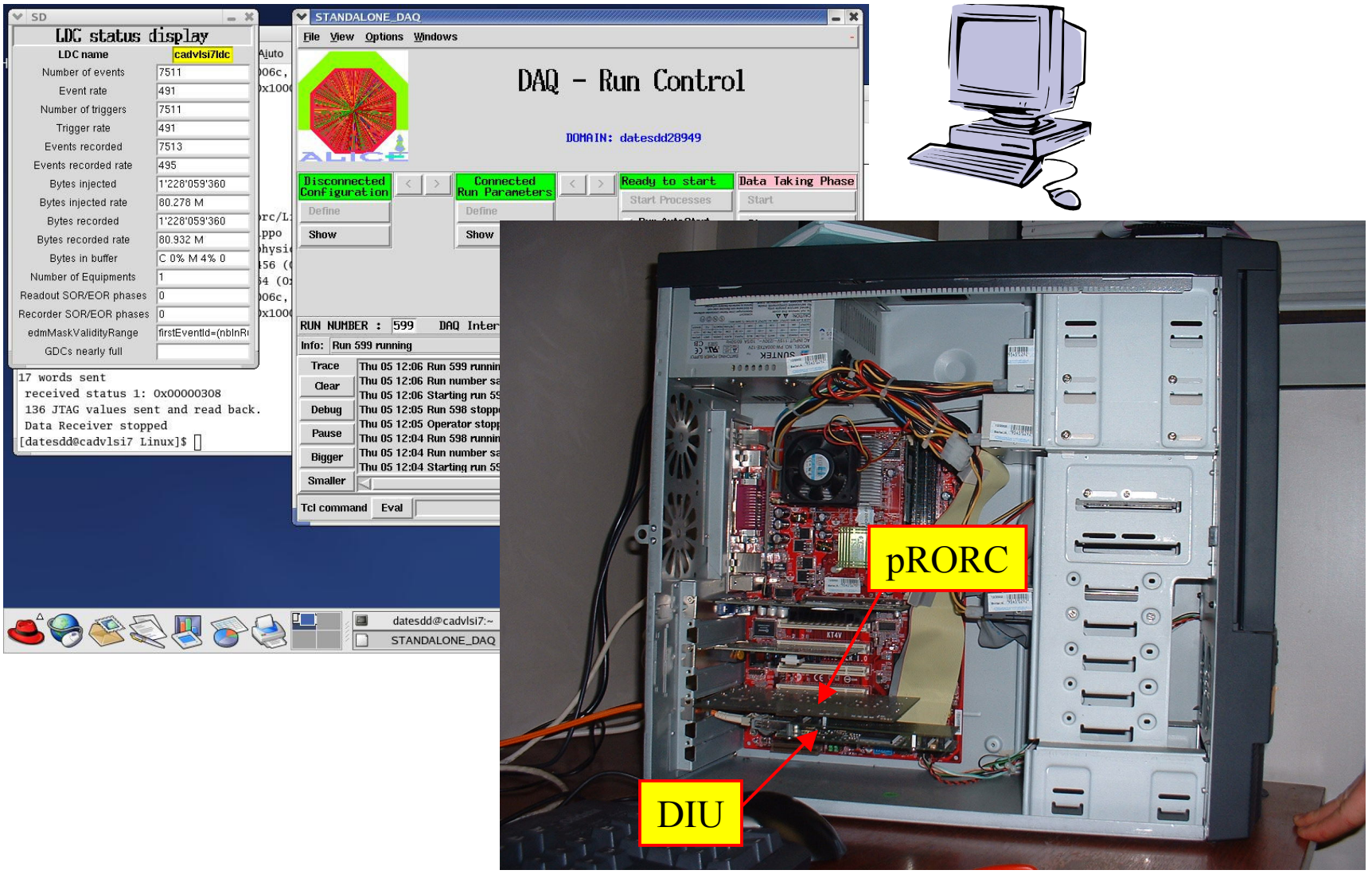
Readout chain implementation in Lab

- CERN DDL installation (SIU + optical fibre + DIU + pRORC + DATE v4.6)

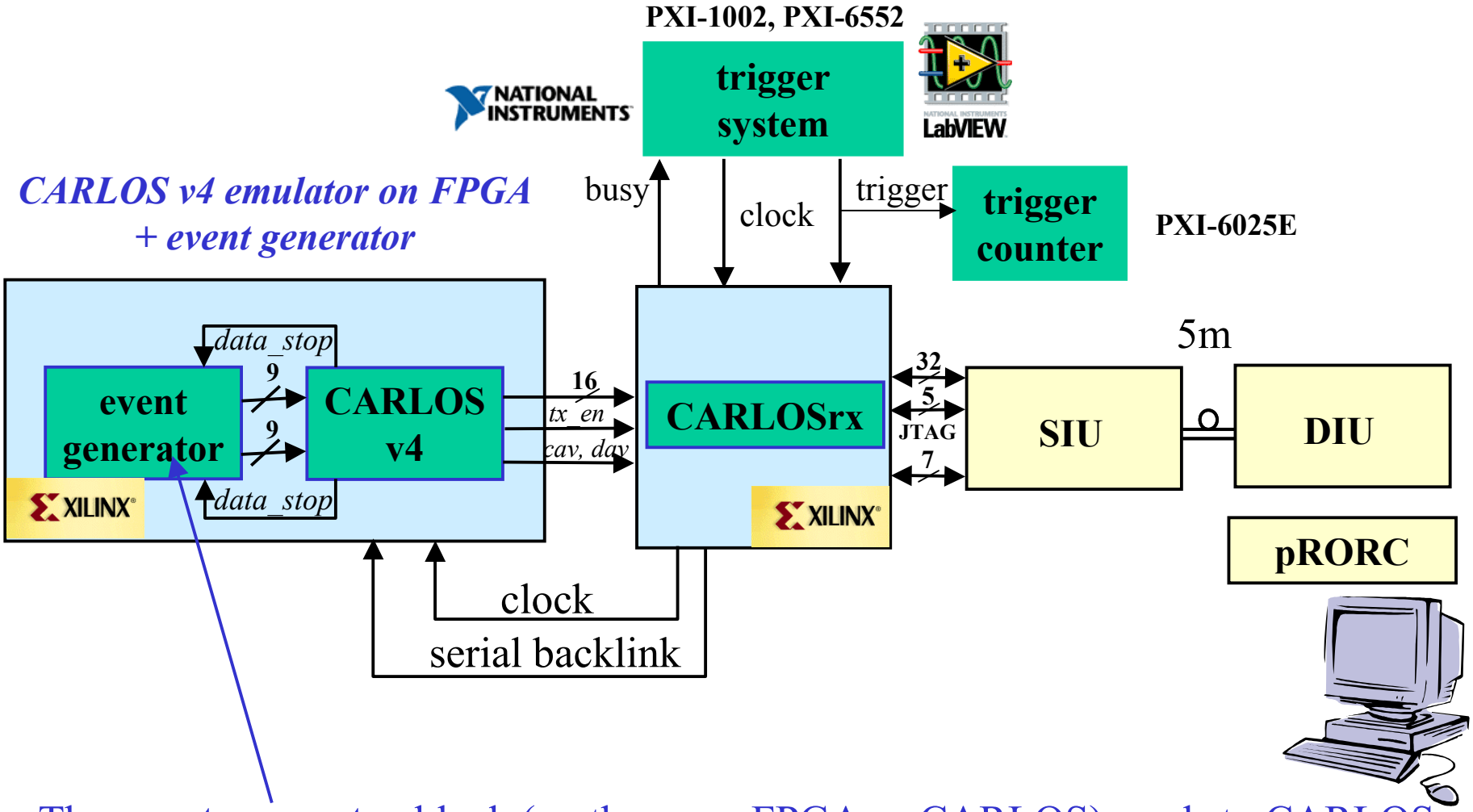


FPGA (Virtex XC2V1000) implementation of the SIU interface for a preliminary test of the DDL

DATE 4.6 & DIU - pRORC

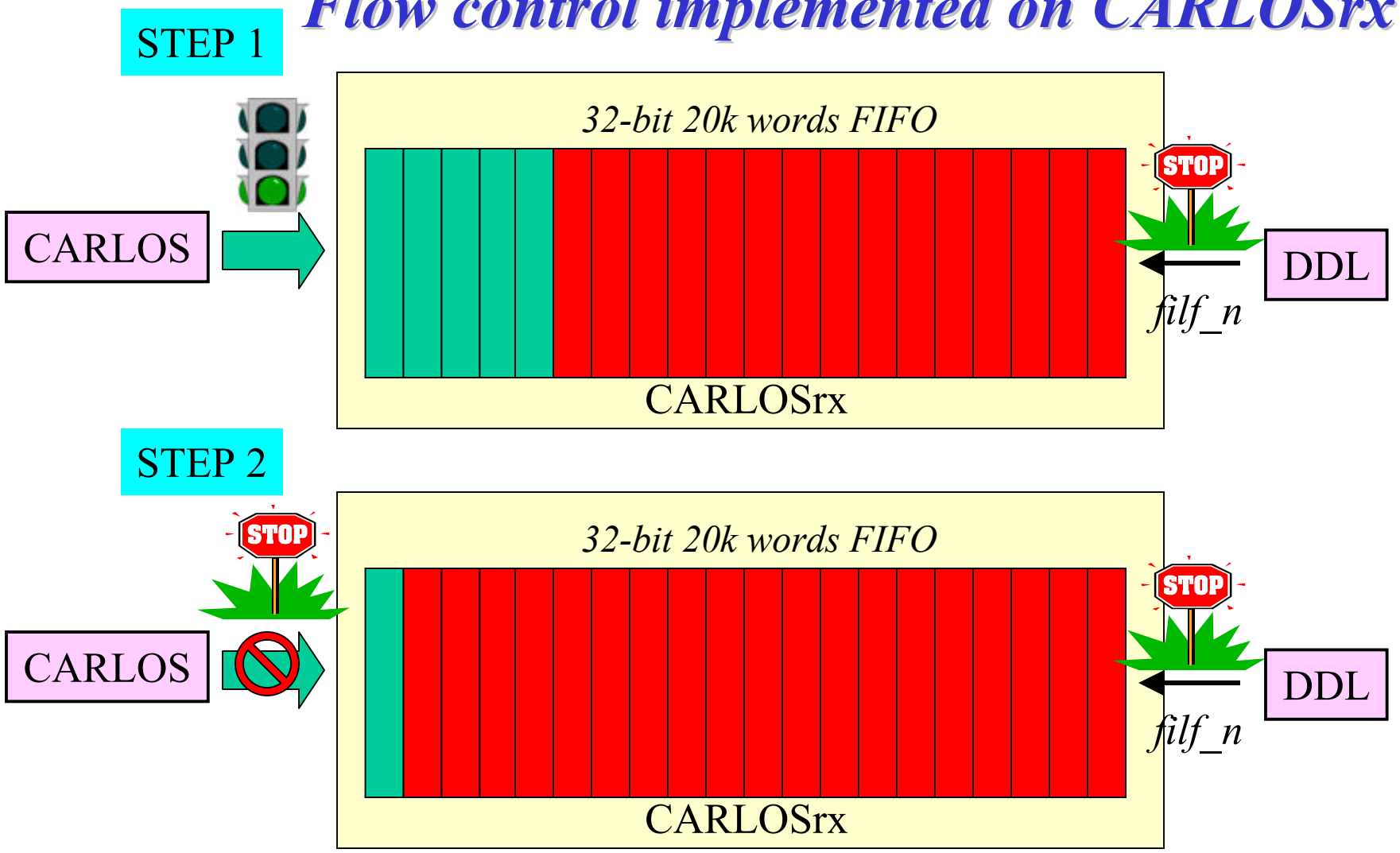


Readout chain implemented in Lab
(before receiving CARLOS v4 ASIC)



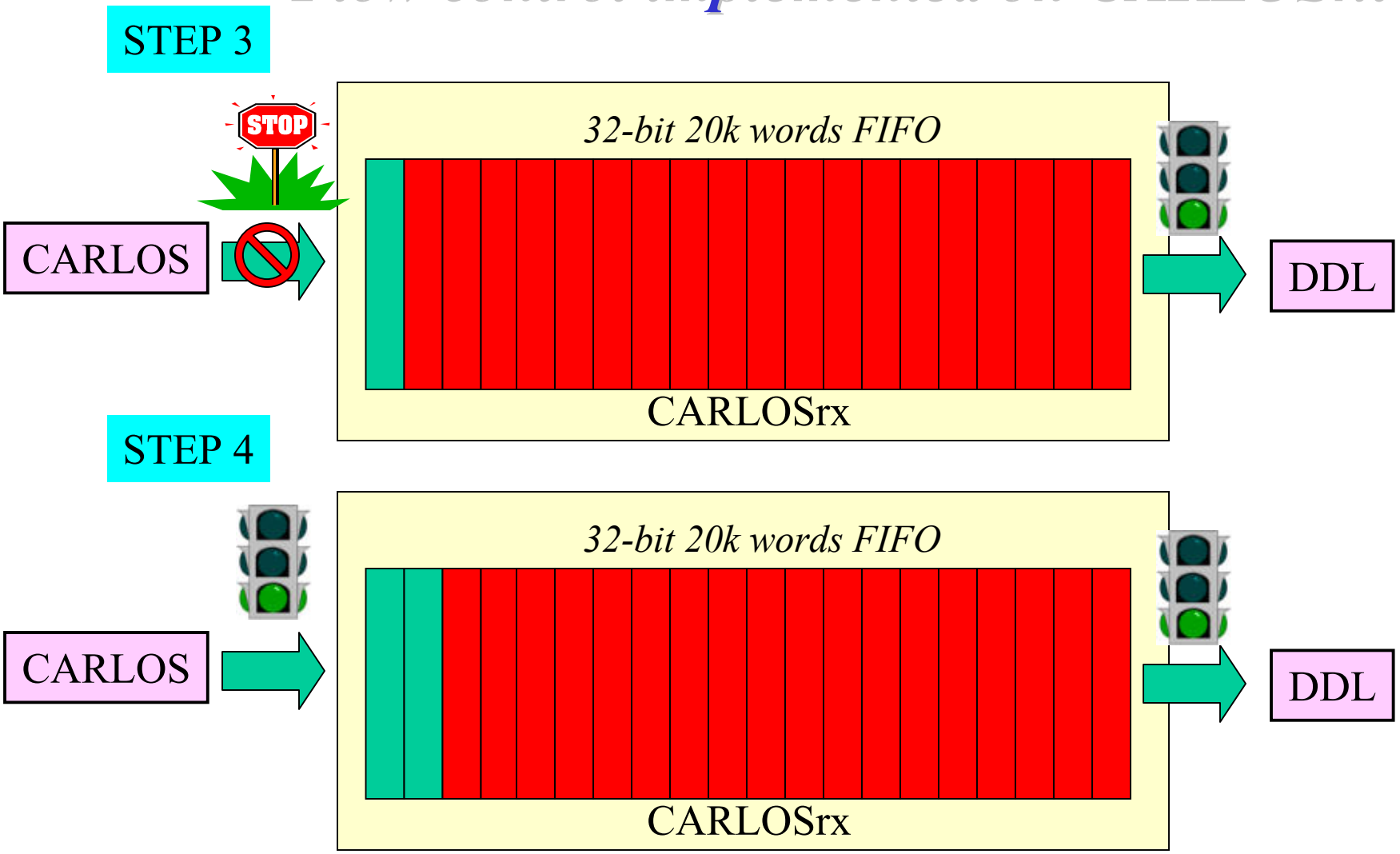
The **event generator** block (on the same FPGA as CARLOS) sends to CARLOS the same event each time it receives a trigger

Flow control implemented on CARLOSrx



CARLOSrx asserts the back-pressure towards CARLOS

Flow control implemented on CARLOSrx

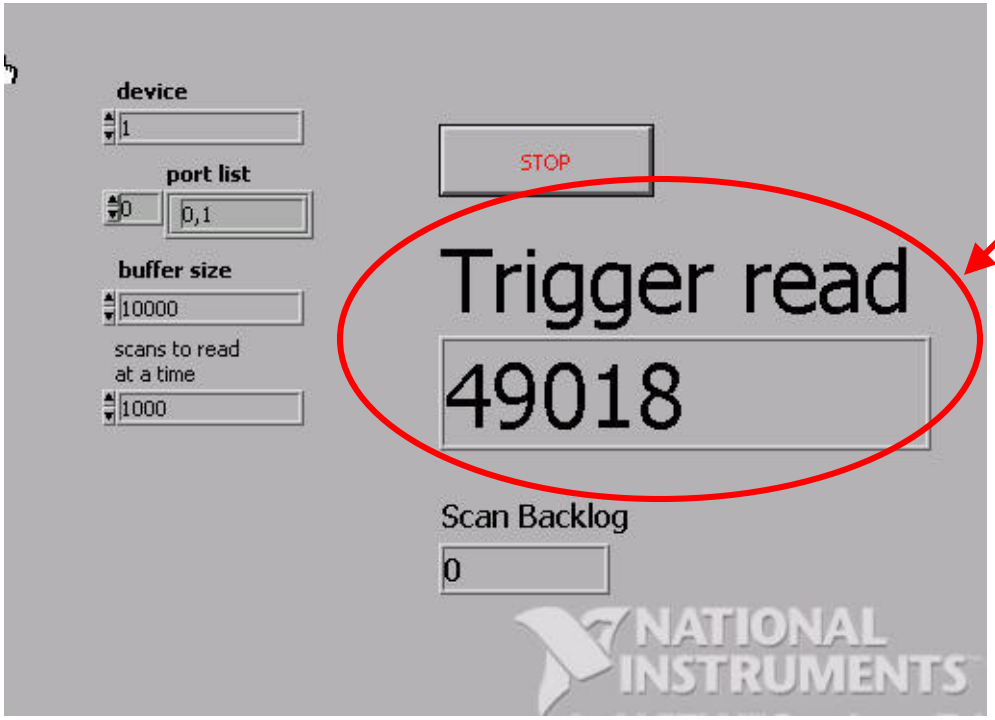


CARLOSrx de-asserts the back-pressure towards CARLOS

Snapshot taken during data acquisition

Number of events recorded

Number of trigger sent

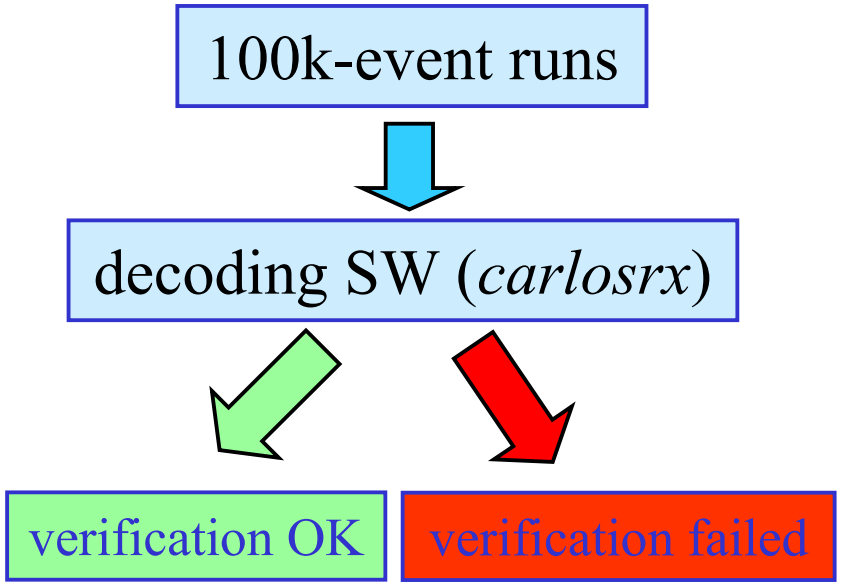


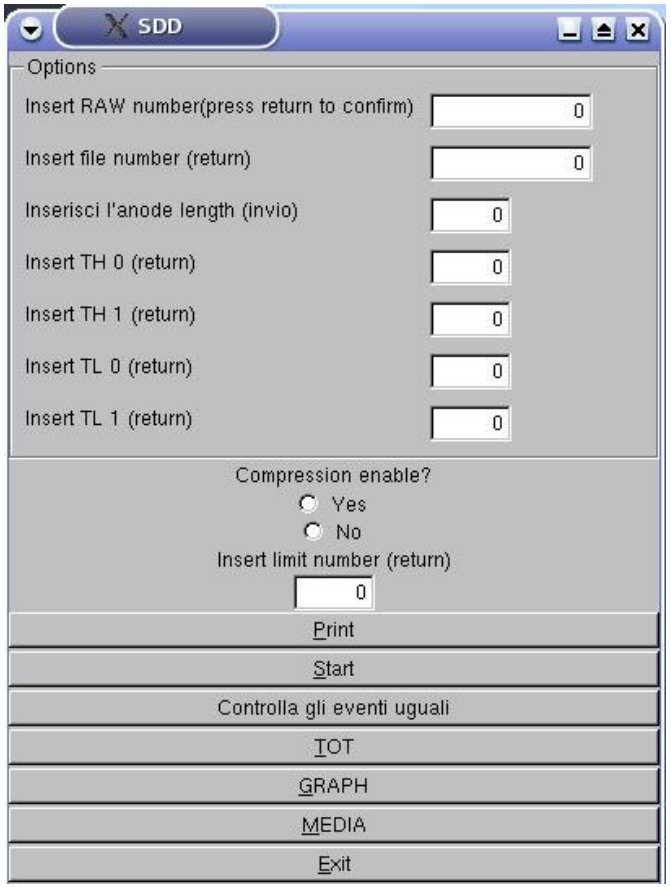
PXI-6025E

LDC status display

LDC name	cadvlsi7ldc
Number of events	49018
Event rate	0
Number of triggers	49018
Trigger rate	0
Events recorded	49020
Events recorded rate	0
Bytes injected	396'911'224
Bytes injected rate	0
Bytes recorded	396'911'224
Bytes recorded rate	0
Bytes in buffer	C 0% M 1% 0
Number of Equipments	1
Readout SOR/EOR phases	0
Recorder SOR/EOR phases	0
edmMaskValidityRange	firstEventId=(nbInR
GDCs nearly full	

Verification step





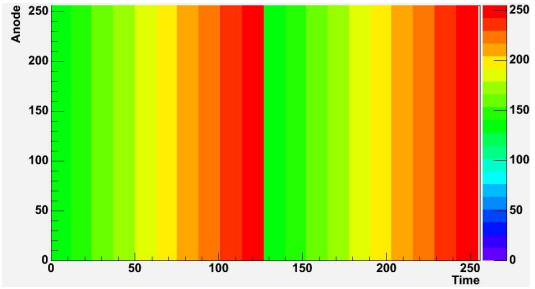
Test features:

- CARLOS programming via JTAG
- Event sizes: 2.5k, 16k e 64k
- Back-pressure of CARLOSrx over CARLOS
- Programmable trigger frequency

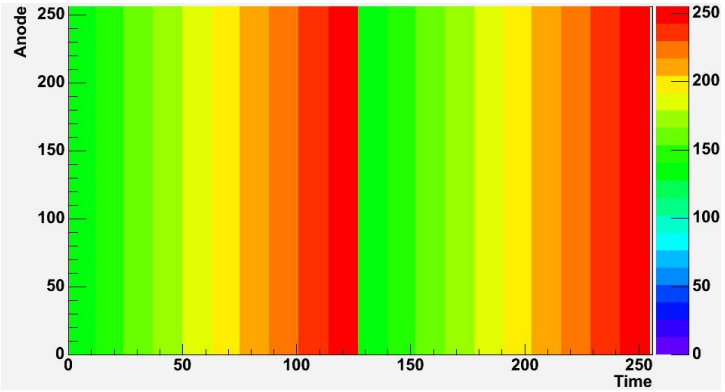
Test of CARLOS v4 (FPGA):

- the interface CARLOS, CARLOSrx, DDL has been successfully tested
- data acquired on PC are correct

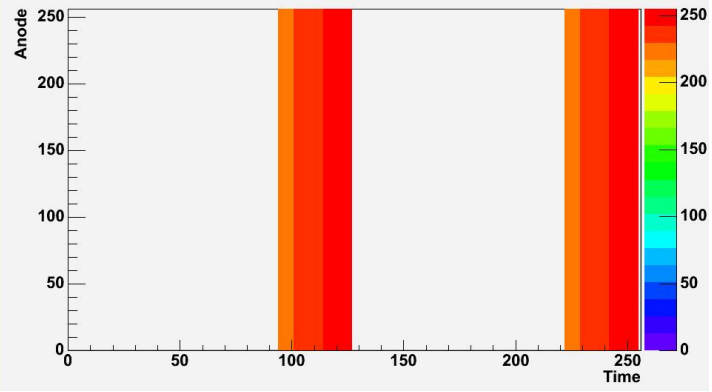
Applying compression to the input pattern



CARLOS – CARLOSrx readout chain

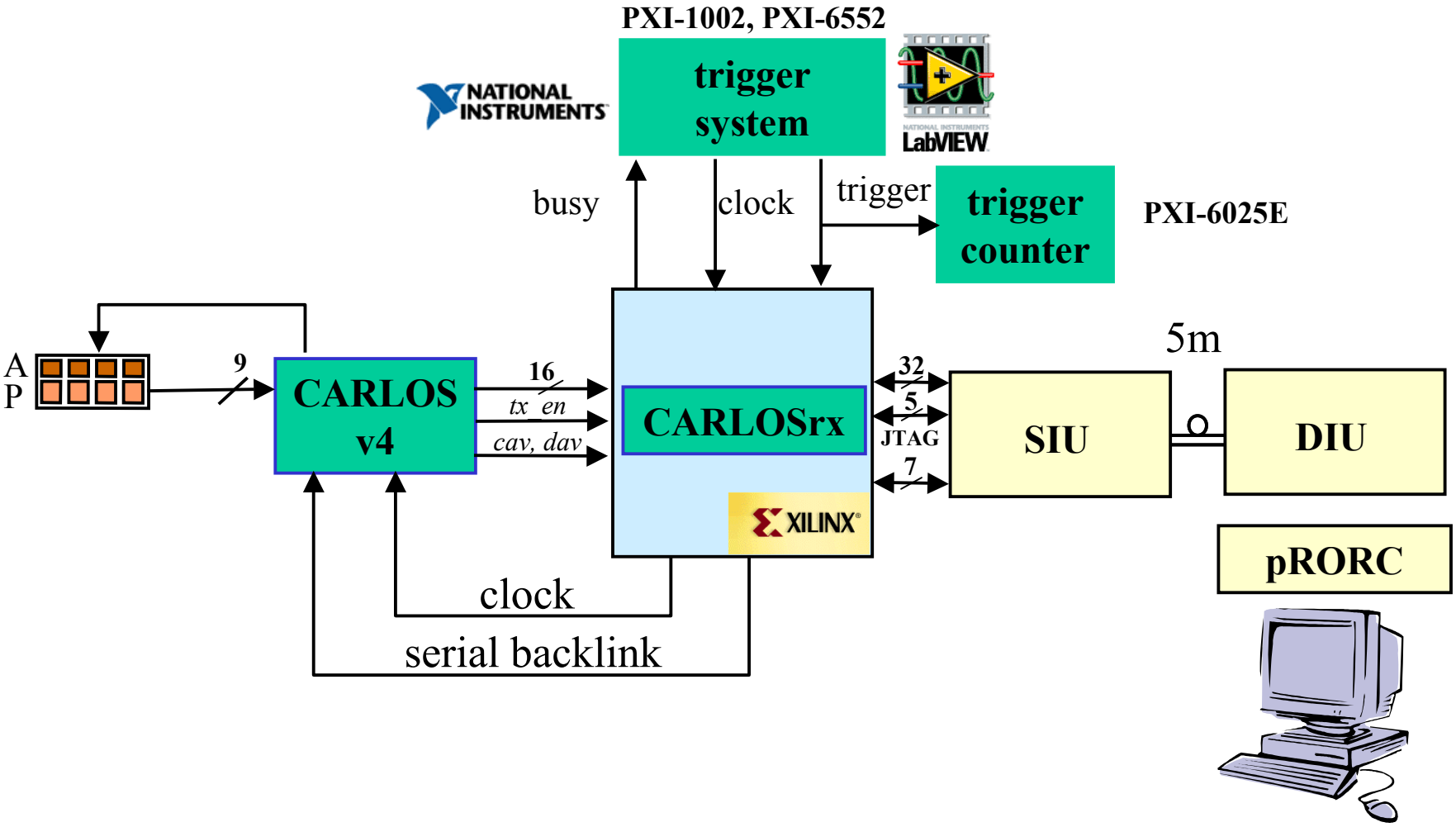


2D compression disabled

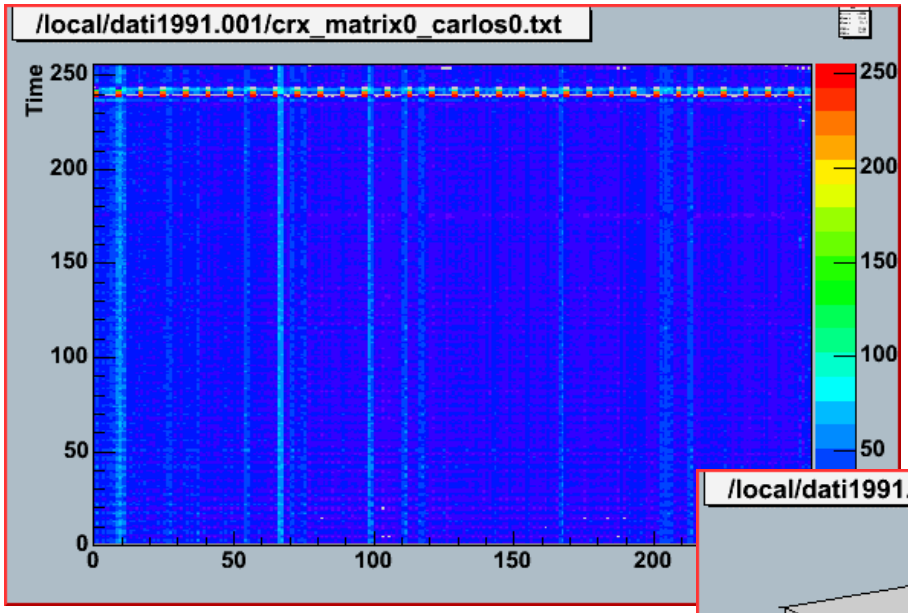


2D compression enabled

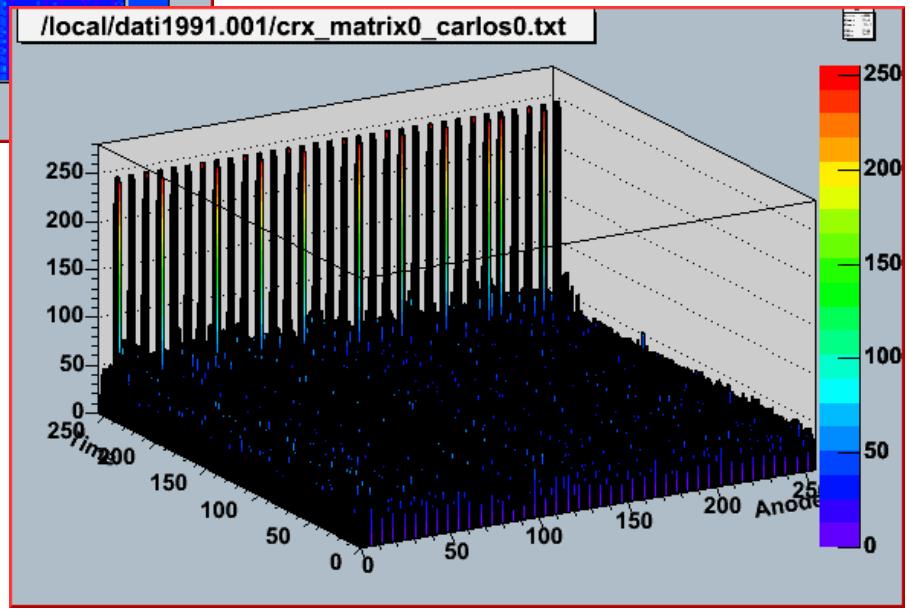
Readout chain with the FEE board and CARLOS v4 ASIC



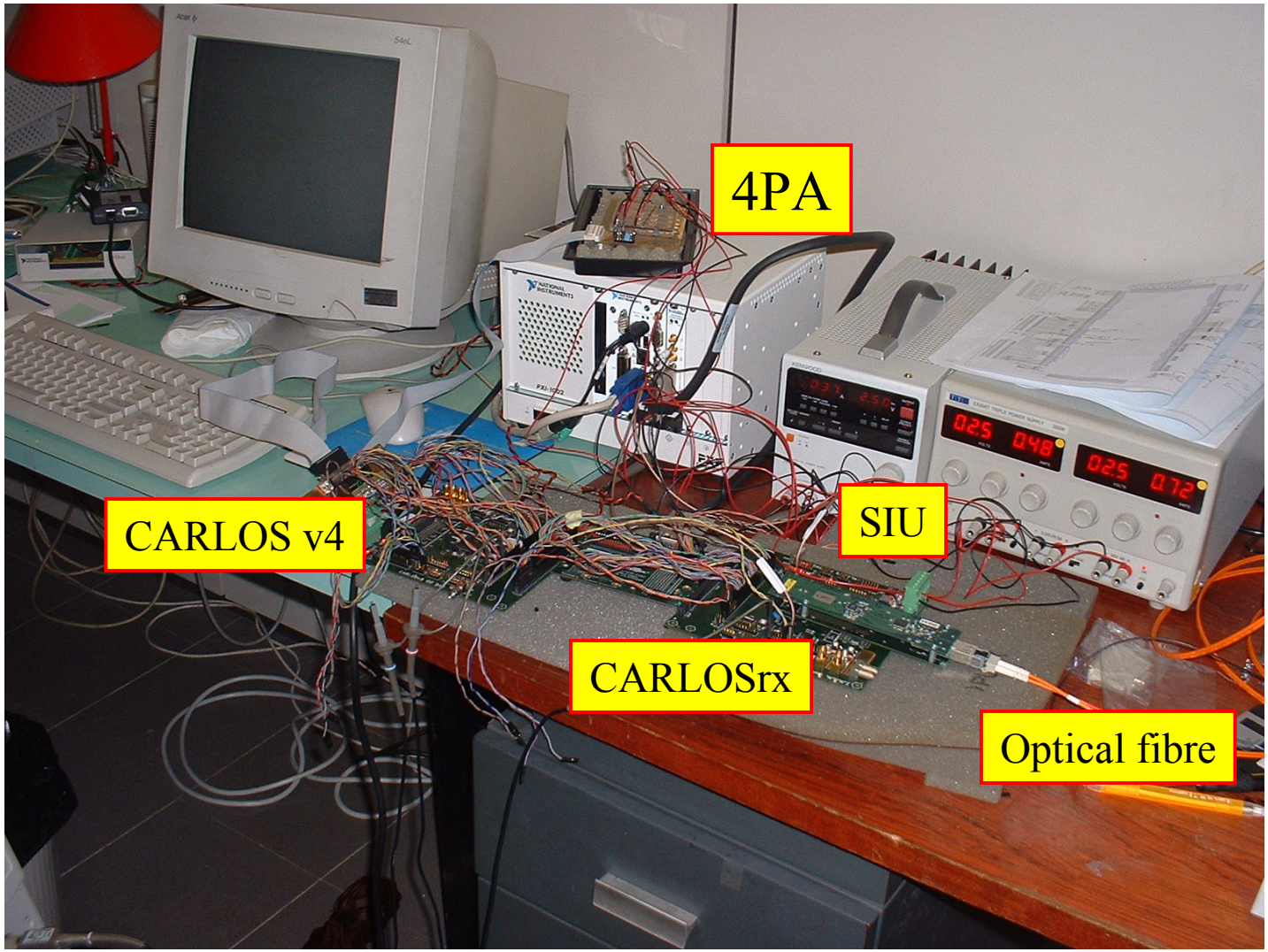
Tests with the FEE board



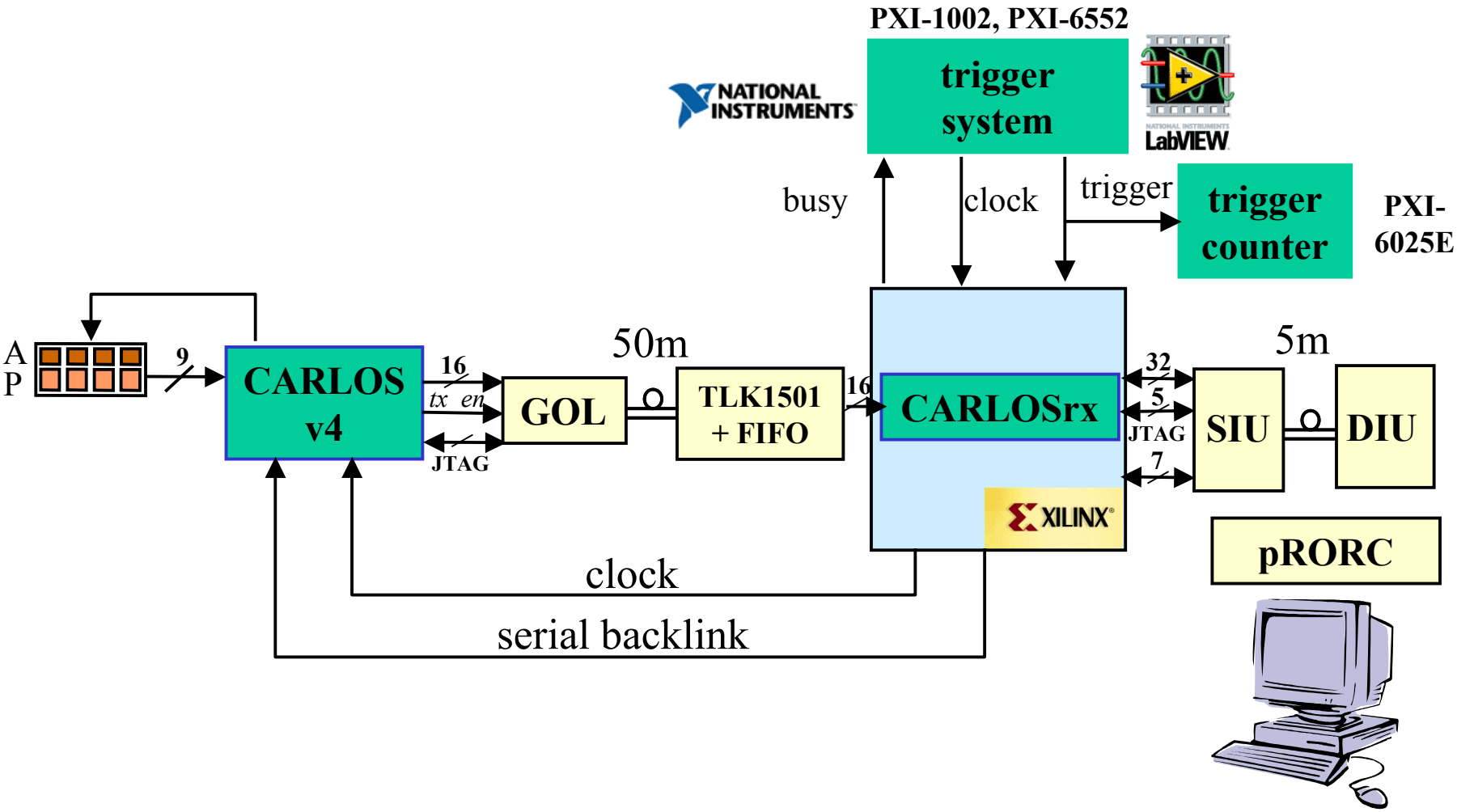
Noise + test pulse with compression disabled



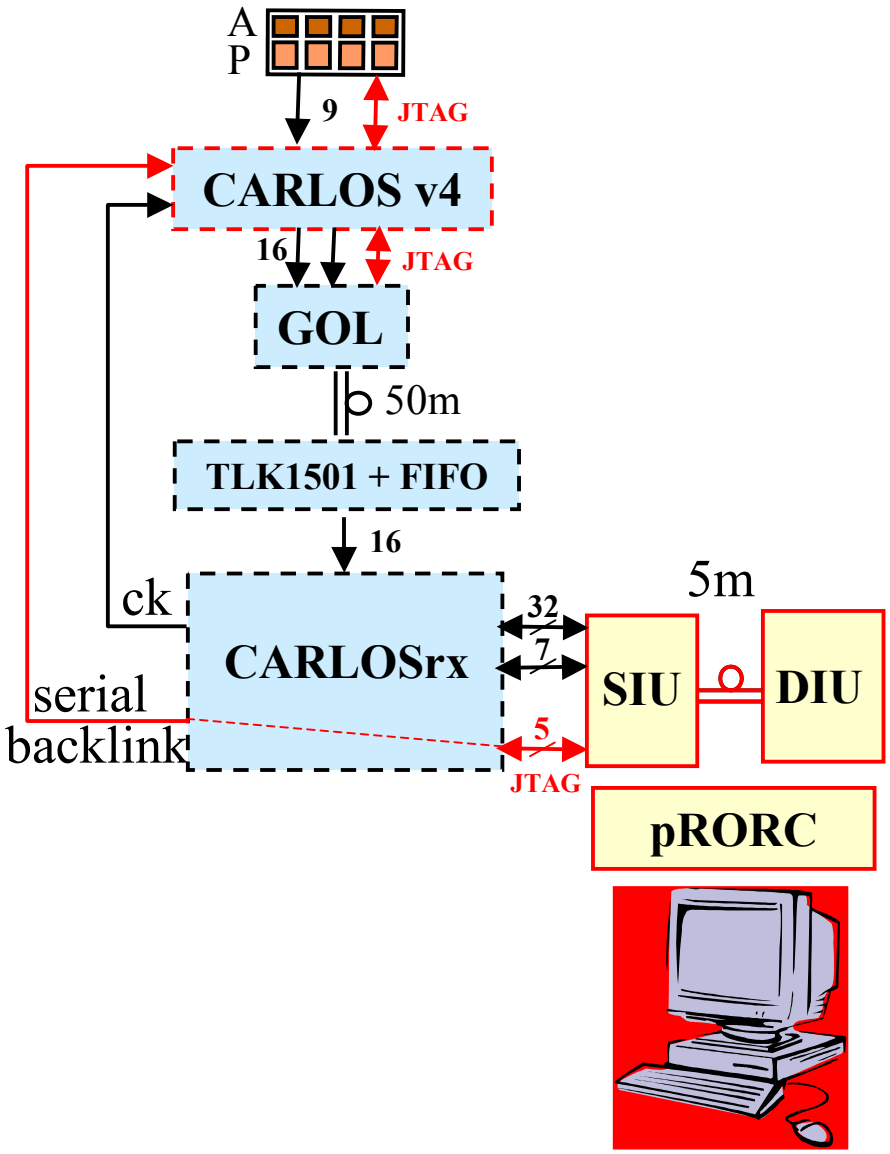
Readout chain (picture)

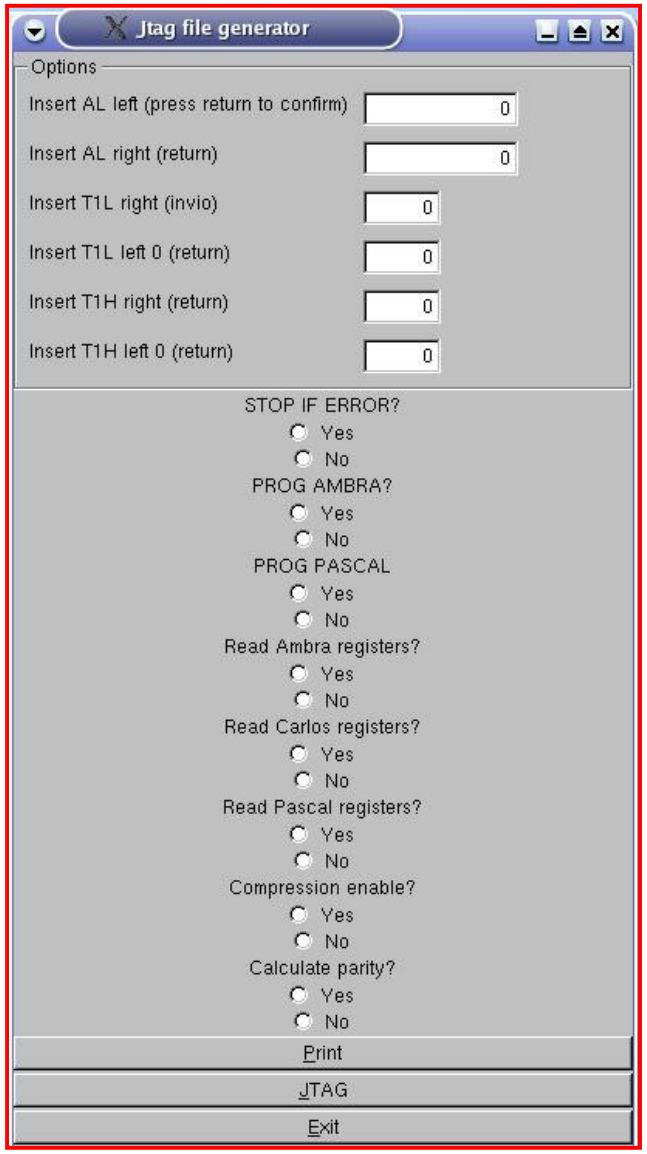


Readout chain with the optical link



Still to come: JTAG file generator for send_jtag





Conclusions

- The DDL, pRORC and DATE allowed us to acquire a very huge amount of data (very soon we had to buy a new 250 GB disk !) and to study very carefully the behaviour of the readout chain.
- We plan to use the DDL, pRORC and DATE acquisition system for the forthcoming tests.

- Attempts to install and use MOOD were not successful.