

	<i>number of SDD module (from 0 to A, only even numbers)</i>			
	FF	FF	FF	00
CARLOSrx	<i>10xxxxxx</i>	physics_run&am_full&PP &TP&active modules	active modules	load trigger
CARLOS	<i>11xxxxxx</i>	<i>address</i>	<i>address</i>	<i>address</i>
	TH ch1	TH ch0	TL ch1	TL ch0
	stop if error	enable 2D	anode length ch1	anode length ch0
	FF	FF	FF	read back
AMBRA ch0 x4	<i>0000xx10</i>	<i>address</i>	<i>address</i>	<i>address</i>
	tx address	read counter	write counter	SOP delay
	<i>mask an. 24-31</i>	<i>mask an. 16-23</i>	<i>mask an. 8-15</i>	<i>mask an. 0-7</i>
	<i>mask an. 56-63</i>	<i>mask an. 48-55</i>	<i>mask an. 40-47</i>	<i>mask an. 32-39</i>
	FF	FF	baseline present	read back
	<i>baseline 3</i>	<i>baseline 2</i>	<i>baseline 1</i>	<i>baseline 0</i>
	...	...	...	...
	<i>baseline 63</i>	<i>baseline 62</i>	<i>baseline 61</i>	<i>baseline 60</i>
PASCAL ch0 x4	<i>0000xx00</i>	<i>address</i>	<i>address</i>	<i>address</i>
	calibration DAC		VREF control DAC	
	ADC full	AM full	gain control	sel cal channels
	FF	FF	FF	read back
AMBRA ch1 x4	<i>0010xx10</i>	<i>address</i>	<i>address</i>	<i>address</i>
	tx address	read counter	write counter	SOP delay
	<i>mask an. 24-31</i>	<i>mask an. 16-23</i>	<i>mask an. 8-15</i>	<i>mask an. 0-7</i>
	<i>mask an. 56-63</i>	<i>mask an. 48-55</i>	<i>mask an. 40-47</i>	<i>mask an. 32-39</i>
	FF	FF	baseline present	read back
	<i>baseline 3</i>	<i>baseline 2</i>	<i>baseline 1</i>	<i>baseline 0</i>
	...	...	...	...
	<i>baseline 63</i>	<i>baseline 62</i>	<i>baseline 61</i>	<i>baseline 60</i>
PASCAL ch1 x4	<i>0010xx00</i>	<i>address</i>	<i>address</i>	<i>address</i>
	calibration DAC		VREF control DAC	
	ADC full	AM full	gain control	sel cal channels
	FF	FF	FF	read back
	FF	FF	FF	11
parametri per	...	...	...	...
il modulo	...	...	...	...
successivo	...	...	...	...
	...	...	...	...
	...	...	...	...
	FF	FF	FF	FF

Numero di risposte JTAG attese per ogni modulo: 4328

*Numero di risposte JTAG attese per ogni modulo (con baseline eq): **12520***

Notes:

- For stopiferror and enable 2D the following encoding has been used:
 - 0 → 00000000
 - 1 → 01111111
- For ADC full and AM full the following encoding has been chosen:
 - 11111111 → full frequency
 - 00000000 → half frequency
- tx_addr:
 - tx_addr is only written during individual addressing
 - only the 2 LSBs are meaningful for tx_addr.

The baseline values are 6-bit numbers. Only the 6 LSBs are taken into account.