

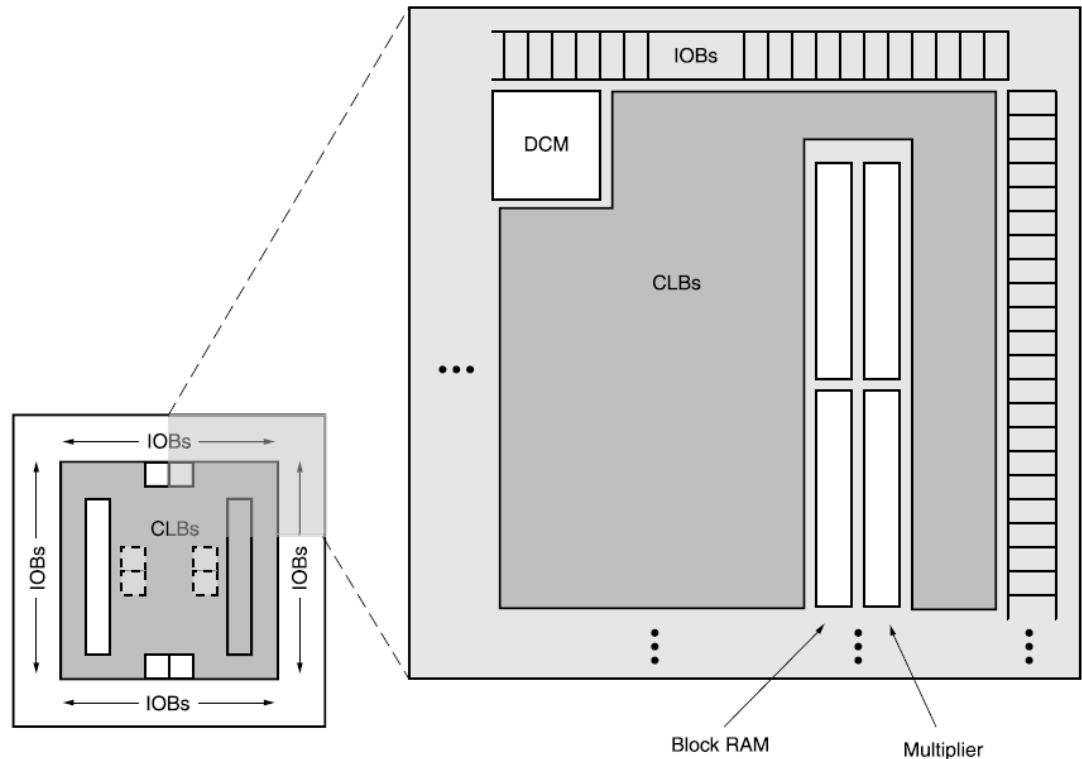
XC3ES500E Spartan3 FPGA

Table 1: Summary of Spartan-3E FPGA Attributes

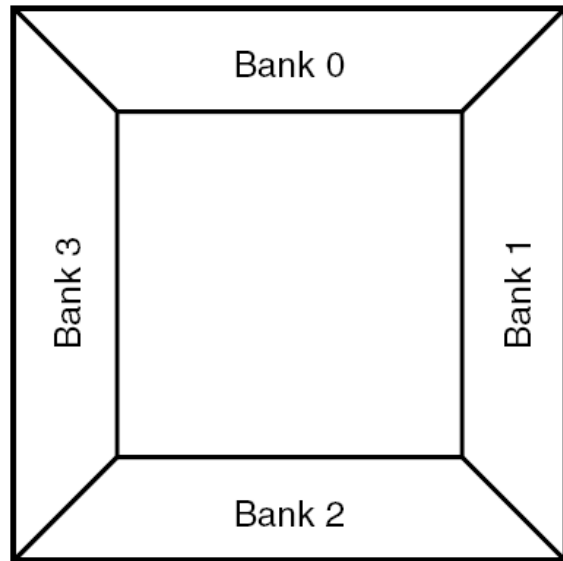
Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits ⁽¹⁾	Block RAM bits ⁽¹⁾	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.



XC3ES500E pinout



I/O Capabilities

The Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. [Table 2](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Spartan-3E FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz, and in some devices, [66 MHz](#)
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

XC3ES500E pinout

Bank 0																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND	TDI	INPUT	I/O L24P_0	INPUT L22P_0	I/O L20N_0	INPUT ↔	I/O	VCCO_0	I/O L12N_0 GCLK7	I/O	I/O	I/O L05P_0	I/O L04N_0	INPUT L02N_0	I/O L01N_0	TCK
B	PROG_B	GND	I/O L25N_0 HSWAP	I/O L24N_0	INPUT L22N_0	I/O L20P_0	VCCAUX	INPUT L13P_0 GCLK9	INPUT L13N_0 GCLK9	I/O L12P_0 GCLK6	I/O VREF_0	VCCAUX	I/O L05N_0 VREF_0	I/O L04P_0	INPUT L02P_0	I/O L01P_0	GND
C	I/O L01P_3	I/O L01N_3	I/O L25P_0	I/O	I/O L23P_0	VCCO_0	I/O L18P_0	INPUT L16P_0	I/O L14P_0 GCLK10	GND	I/O L08P_0	INPUT L07P_0	VCCO_0	I/O L03N_0 VREF_0	INPUT	TDO	I/O L24N_1 LDC2
D	I/O L02P_3	I/O L02N_3 VREF_3	INPUT	I/O	I/O L23N_0 VREF_0	I/O L21P_0	I/O L18N_0 VREF_0	INPUT L16N_0	I/O L14N_0 GCLK11	I/O L11P_0 GCLK4	I/O L08N_0	INPUT L07N_0	INPUT ↔	I/O L03P_0	TMS	I/O L23N_1 LDC0	I/O L23P_1 HDG
E	I/O L03N_3	I/O L03P_3	I/O L04N_3	I/O L04P_3	VCCINT	I/O L21N_0	I/O L19N_0 VREF_0	I/O L17P_0	I/O L15P_0	I/O L11N_0 GCLK5	I/O L08P_0	I/O L06N_0	I/O	VCCINT	I/O L22P_1	I/O L22N_1	INPUT ↔
F	I/O L05P_3	I/O L05N_3	VCCO_3	INPUT ↔	INPUT	VCCINT	I/O L19P_0	I/O L17N_0	I/O L15N_0	INPUT L10N_0	I/O L08N_0	I/O L06P_0	VCCINT	I/O L20N_1	I/O L21P_1	VCCO_1	I/O L19N_1
G	INPUT	VCCAUX	I/O L06P_3	I/O L06N_3 VREF_3	I/O L07N_3	I/O L07P_3	GND	VCCO_0	I/O	INPUT L10N_0	VCCO_0	GND	I/O L20N_1	I/O L20P_1	I/O L18P_1	I/O L18N_1	VCCAUX
H	I/O L10N_3	I/O L10P_3	I/O L09N_3	I/O L09P_3	I/O L08N_3	I/O L08P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	I/O L17P_1	I/O L17N_1	I/O L16P_1	I/O L16N_1 A0
J	I/O L12P_3 LHCLK2	I/O L12N_3 LHCLK3 IRDY2	GND	I/O L14N_3 LHCLK1	I/O L14P_3 LHCLK0	INPUT VREF_3	INPUT	GND	X			GND	I/O L15P_1 A2	I/O L15N_1 A1	I/O L14P_1 A0 RHCLK7	I/O L13N_1 A3 RHCLK5	I/O L13P_1 A4 RHCLK4 IRDY1
K	VCCO_3	INPUT	I/O L13P_3 LHCLK5 IRDY3	I/O L13N_3 LHCLK6	I/O L14N_3 LHCLK7	I/O L14P_3 LHCLK6	INPUT	GND				GND	I/O L11N_1 A5 RHCLK1	I/O L11P_1 A6 RHCLK0	I/O L10N_1 A7 RHCLK3 TROY1	GND	INPUT
L	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	I/O L17N_3 VREF_3	I/O L17P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	INPUT	I/O L09N_1 A11	I/O L09P_1 A12	I/O L10N_1 VREF_1
M	INPUT	VCCAUX	I/O L18P_3	I/O L18N_3	I/O L19P_3	I/O L19N_3	GND	VCCO_2	I/O L16P_2 GCLK13	I/O L16N_2 M0	VCCO_2	GND	I/O L05N_1 VREF_1	I/O L05P_1	I/O L07P_1	I/O L07N_1	VCCAUX
N	INPUT	INPUT	VCCO_3	I/O L20P_3	I/O L20N_3	VCCINT	I/O L07P_2	I/O L09N_2	I/O L16P_2 GCLK12	I/O L16N_2 DM0	I/O L18N_2	I/O L21P_2	VCCINT	I/O L04N_1	I/O L04P_1	VCCO_1	INPUT
P	I/O L21N_3	I/O L21P_3	I/O L22N_3	I/O L22P_3	VCCINT	I/O L08N_2	I/O L07N_2	I/O L08P_2	I/O L15N_2 D1 GCLK9	I/O L18P_2	I/O L18N_2	I/O L21N_2	I/O L23P_2 A23	VCCINT	INPUT ↔	I/O	I/O L06P_1
R	INPUT	I/O L23N_3	I/O L23P_3	INPUT VREF_3 ↔	I/O L04P_2	I/O L05P_2	INPUT L08N_2	I/O L10P_2	I/O L15P_2 D2 GCLK2	I/O	I/O L20N_2	I/O L22N_2 A22	I/O L24N_2 A20	I/O L03P_1	I/O L03N_1 VREF_1	INPUT	I/O L03P_1 A14
T	I/O L24N_3	I/O L24P_3	I/O L01N_2 INIT_B	I/O L03N_2 MCS1 CS1_B	I/O L04N_2	VCCO_2	INPUT L08P_2	I/O L10N_2	GND	INPUT L14N_2 GCLK1	INPUT L17P_2	I/O L20P_2	VCCO_2	I/O L24P_2 A21	I/O VREF_2	I/O L23P_2 VS1 A18	I/O L01N_1 A15
U	INPUT	GND	I/O L01P_2 CS0_B	I/O L03P_2 DOUT BUSY	I/O VREF_2	INPUT ↔	VCCAUX	INPUT L11P_2	I/O L16P_2 D4 GCLK14	I/O L14P_2 ROWB_B GCLK0	INPUT L17N_2	VCCAUX	INPUT ↔	INPUT L23N_2	I/O L25N_2 CCLK	GND	I/O L01P_1 A16
V	GND	INPUT	INPUT L02N_2	INPUT L02P_2	I/O L06P_2	I/O L06N_2 VREF_2	I/O	INPUT L11N_2 VREF_2	I/O L15N_2 GCLK15	VCCO_2	I/O M1	I/O L19P_2	I/O L19N_2 VREF_2	INPUT L23P_2	INPUT L25P_2 VS2 A19	INPUT	DONE
Bank 2																	

- 102-120** I/O: Unrestricted, general-purpose user I/O
- 47-48** INPUT: Unrestricted, general-purpose input pin
- 2** CONFIG: Dedicated configuration pins
- 18** N.C.: Not connected. Only the XC3S500E has these pins (♦).
- 46** DUAL: Configuration pin, then possible user-I/O
- 16** CLK: User I/O, input, or global buffer input
- 4** JTAG: Dedicated JTAG port pins
- 28** GND: Ground
- 20-21** VREF: User I/O or input voltage reference for bank
- 20** VCCO: Output voltage supply for bank
- 8** VCCINT: Internal core supply voltage (+1.2V)
- 8** VCCAUX: Auxiliary supply voltage (+2.5V)

VGA

PS2

RS232

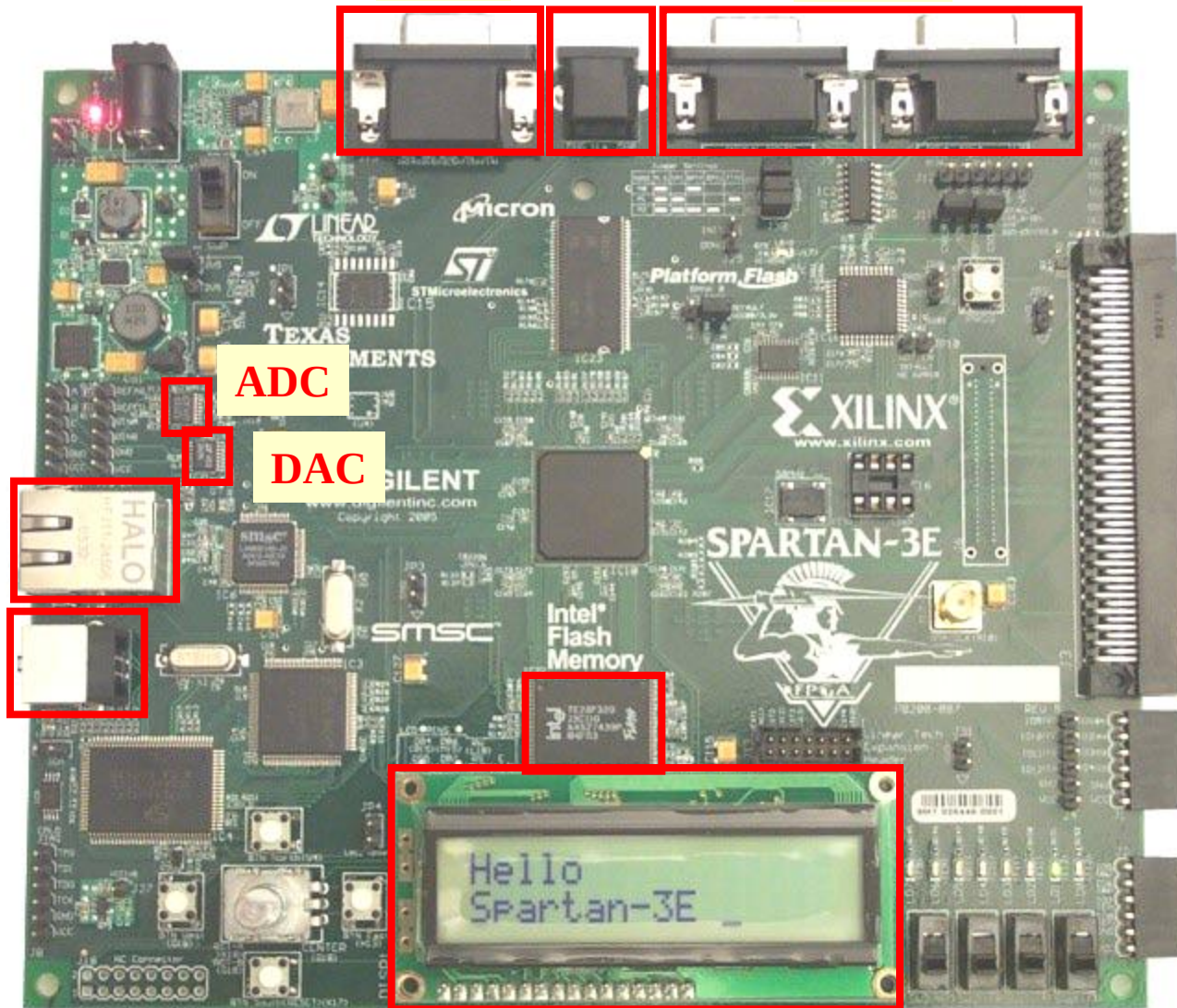
ADC

DAC

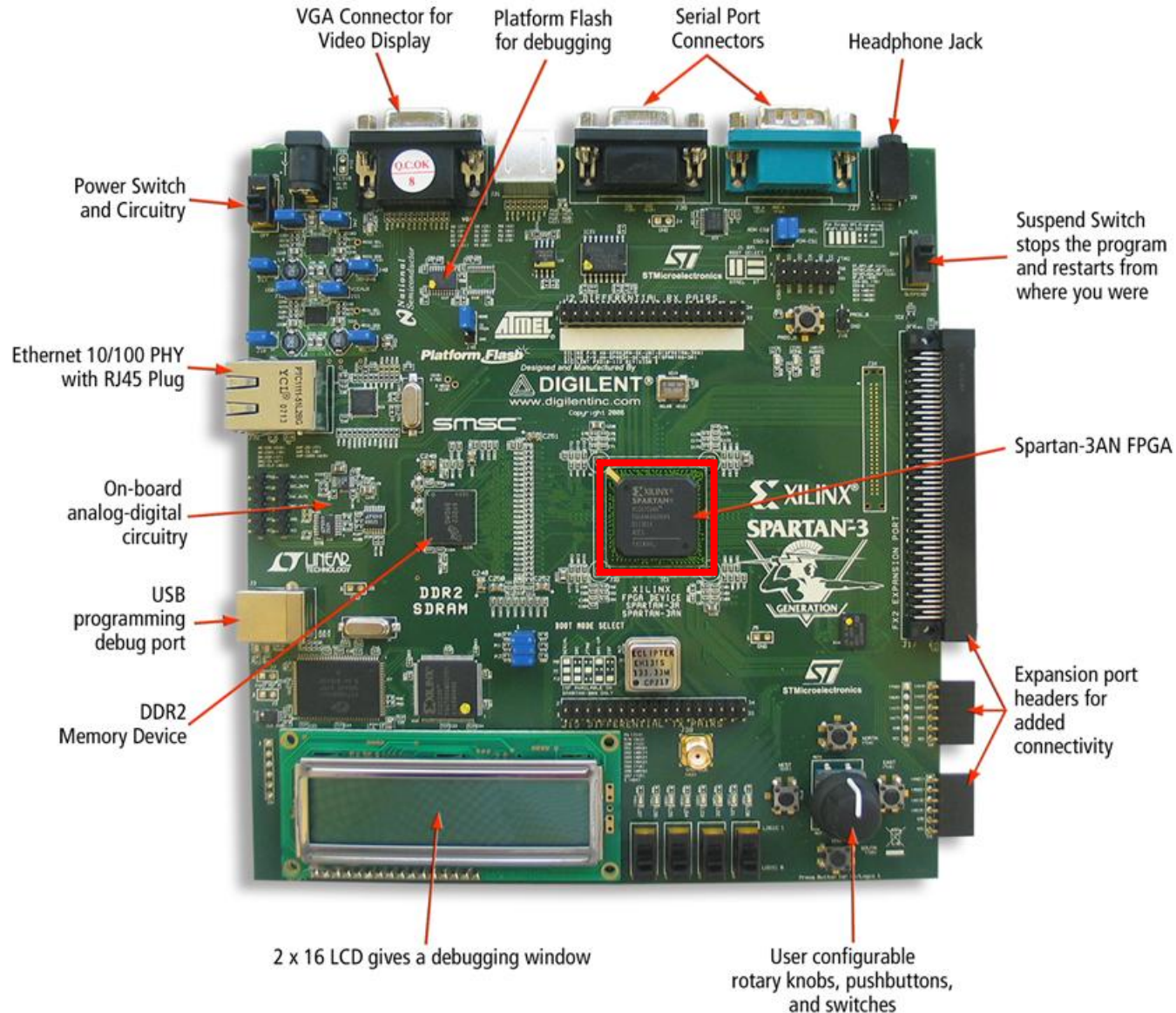
Ethernet

USB

LCD screen

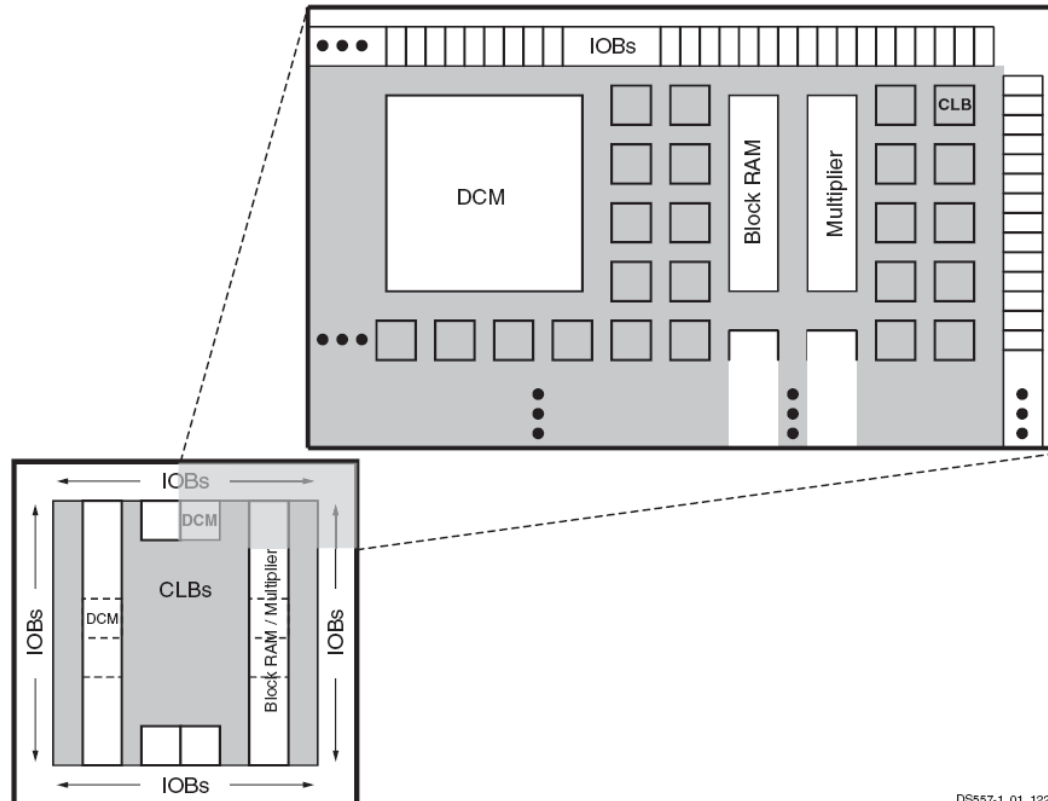


Xilinx demo board: XC3ES700AN Spartan3AN FPGA



XC3ES700AN Spartan3 FPGA

Device	System Gates	Equivalent Logic Cells	CLBs	Slices	Distributed RAM Bits ⁽¹⁾	Block RAM Bits ⁽¹⁾	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs	Bitstream Size ⁽¹⁾	In-System Flash Bits
XC3S50AN	50K	1,584	176	704	11K	54K	3	2	108	50	427K	1M
XC3S200AN	200K	4,032	448	1792	28K	288K	16	4	195	90	1,168K	4M
XC3S400AN	400K	8,064	896	3,584	56K	360K	20	4	311	142	1,842K	4M
XC3S700AN	700K	13,248	1472	5,888	92K	360K	20	8	372	165	2,669K	8M
XC3S1400AN	1400K	25,344	2816	11,264	176K	576K	32	8	502	227	4,644K	16M

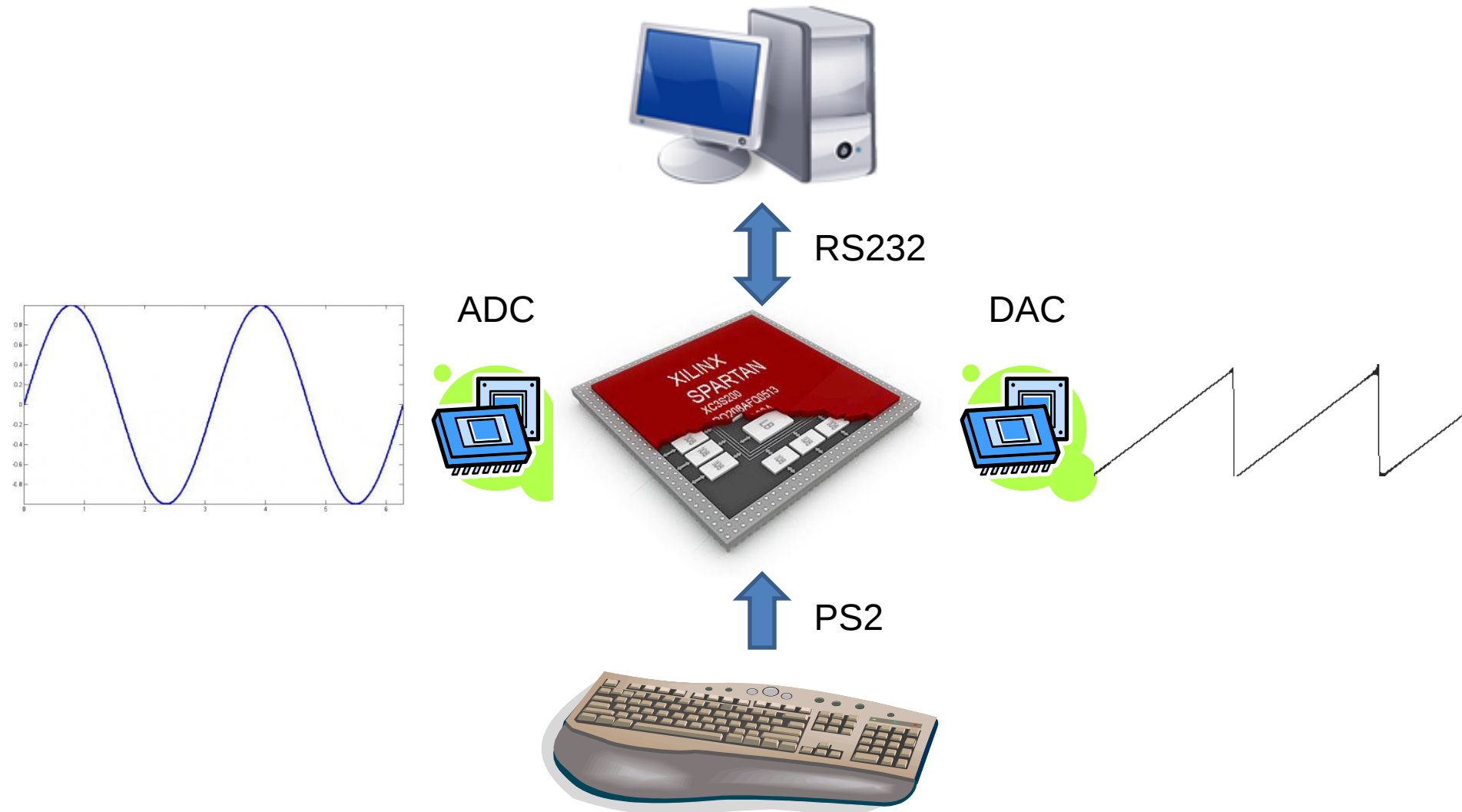


XC3S700AN-4FGG484C

		Bank 0											Bank 0												
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22		
Bank 2	A	GND	IO L338_0 PUDC_0	IO L337_0	IO L319_0	IO L281_0	IO L269_0	IO L229_0	IO L217_0	IO L189_0 GOLK0	IO L167_0 GOLK0	IO L138_0	IO L126_0 VREF_0	IO L123_0	IO L109_0	IO L089_0	IO L069_0	IO L039_0	TCK	GND			A		
	B	IO L069_0	IO L369_0 VREF_0	IO L338_0	IO L319_0	VCC0_0	IO L289_0	GND	IO L259_0	IO L247_0	VCC0_0	IO L197_0 GOLK0	GND	IO L189_0	VCC0_0	IO L159_0	GND	IO L109_0	VCC0_0	IO L089_0 VREF_0	IO L059_0	IO L459_0 A20	IO L469_0 A20	B	
	C	IO L019_0	IO L029_0	GND	VREF_0	IO L329_0	IO L289_0	IO L279_0	IO L259_0	IO L249_0 VREF_0	IO L219_0 GOLK0	IO L199_0 GOLK0	IO L179_0 GOLK0	IO L159_0	IO L139_0	IO L119_0	IO L099_0	IO L079_0	IO L059_0	GND	IO L449_0 A21	IO L449_0 A20	C		
	D	IO L069_0	IO L019_0	IO L039_0	TMS	IO L329_0	IO L289_0	IO L279_0	IO L269_0	GND	IO L239_0	IO L339_0 GOLK0	VCCAUX	IO L199_0	GND	IO L119_0	IO L089_0	IO L079_0	IO L019_0	IO L029_0 VREF_0	IO L429_0	IO L439_0	IO L419_0	D	
	E	IO L069_0	VCC0_0	IO L319_0	IO L039_0	VCCAUX	IO L359_0	IO L349_0	INPUT	IO L339_0	IO L339_0 GOLK1	IO L319_0 GOLK1	IO L199_0	IO L149_0	IO L099_0	IO L049_0	INPUT	IO L019_0	VCCAUX	TDO	IO L389_0	VCC0_0	IO L419_0	E	
	F	IO L129_0	IO L129_0	IO L089_0	IO L079_0	TDI	GND	IO L359_0	IO L349_0	INPUT	GND	INPUT	IO L149_0	VCC0_0	IO L099_0	IO L049_0	INPUT	GND	IO L409_0	IO L409_0	IO L389_0	IO L349_0 A15	IO L349_0 A15	F	
	G	IO L129_0	GND	IO L139_0	IO L089_0	IO L059_0	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	IO L409_0 A25	IO L409_0 A24	IO L369_0	IO L369_0	GND	IO L339_0 A15	IO L339_0 A15	G
	H	IO L169_0	IO L169_0	IO L149_0	IO L149_0	IO L099_0	IO L099_0	INPUT	IO L049_0 VREF_0	INPUT	INPUT	VCCAUX	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	IO L389_0	IO L379_0	IO L359_0 A17	IO L339_0 A16	IO L339_0 A14	H	
	J	IO L179_0 VREF_0	VCC0_0	IO L179_0	GND	IO L109_0	VCC0_0	INPUT	INPUT	GND	VCCINT	GND	VCCINT	GND	VCCINT	INPUT	IO L439_0 VREF_0	INPUT	VCC0_0	IO L379_0	GND	IO L329_0 A13	IO L329_0 A12	IO L329_0 A11	J
	K	IO L339_0 VREF_0	IO L329_0	IO L329_0	IO L189_0	IO L189_0	IO L159_0	INPUT	INPUT	VCCINT	GND	VCCINT	GND	VCCINT	INPUT	IO L359_0 VREF_0	IO L319_0	IO L309_0	IO L299_0 VREF_0	IO L259_0 VREF_0	VCC0_0	IO L239_0 A10	IO L239_0 A10	K	
	L	IO L229_0 VREF_0	GND	IO L219_0 VREF_0	VCCAUX	IO L219_0 VREF_0	GND	INPUT	INPUT	INPUT	GND	VCCINT	GND	VCCINT	GND	VCCINT	INPUT	IO L319_0	IO L279_0	GND	IO L289_0 VREF_0	IO L229_0 VREF_0	IO L219_0 VREF_0	IO L219_0 VREF_0	L
	M	IO L349_0 VREF_0	IO L349_0 VREF_0	IO L329_0 VREF_0	IO L329_0 VREF_0	IO L329_0 VREF_0	INPUT	INPUT	INPUT	INPUT	VCCINT	GND	VCCINT	GND	VCCINT	GND	INPUT	IO L319_0 VREF_0	IO L299_0	VCCAUX	IO L349_0 VREF_0	GND	IO L319_0 VREF_0	IO L319_0 VREF_0	M
	N	IO L299_0 VREF_0	VCC0_0	IO L269_0	IO L309_0	IO L319_0	IO L319_0	IO L359_0	IO L279_0	IO L279_0	VCCINT	GND	VCCINT	GND	VCCINT	INPUT	IO L189_0 VREF_0	IO L189_0 A2	IO L189_0 A2	IO L189_0 A2	IO L189_0 A2	IO L189_0 A2	IO L189_0 A2	N	
	P	IO L269_0	IO L269_0	IO L269_0	GND	IO L299_0	VCC0_0	INPUT	INPUT	INPUT	GND	GND	VCCAUX	INPUT	VCCINT	GND	INPUT	IO L179_0 VREF_0	VCC0_0	IO L159_0	GND	IO L159_0 VREF_0	IO L159_0 VREF_0	P	
	R	IO L329_0	IO L329_0	IO L329_0	IO L329_0	IO L349_0	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	IO L049_0 VREF_0	IO L049_0 VREF_0	IO L029_0 VREF_0	IO L029_0 VREF_0	IO L129_0 VREF_0	IO L129_0 VREF_0	IO L149_0	IO L149_0	R	
	T	IO L389_0 VREF_0	GND	IO L369_0	IO L349_0	IO L409_0	INPUT	INPUT	N.C.	INPUT	INPUT	INPUT	GND	INPUT	INPUT	INPUT	INPUT	IO L039_0 VREF_0	IO L039_0 VREF_0	IO L129_0 VREF_0	IO L119_0	GND	IO L119_0	T	
	U	IO L379_0	IO L379_0	IO L419_0	IO L419_0	IO L409_0	GND	N.C.	INPUT	VCC0_0	INPUT	IO L179_0 GOLK1	IO L169_0 GOLK1	IO L169_0 GOLK1	IO L169_0 GOLK1	IO L139_0	IO L139_0	IO L139_0	IO L109_0	IO L109_0	IO L099_0	IO L099_0	IO L099_0	U	
	V	IO L389_0	VCC0_0	IO L349_0	IO L439_0	IO L439_0	VCCAUX	IO L019_0 VREF_0	INPUT	INPUT	INPUT	IO L139_0 GOLK1	IO L139_0 GOLK1	IO L139_0 GOLK1	IO L139_0 GOLK1	IO L139_0	IO L139_0	IO L139_0	VCCAUX	IO L069_0	IO L069_0	VCC0_0	IO L079_0	V	
	W	IO L439_0	IO L429_0	IO L419_0	IO L029_0 VREF_0	IO L019_0 VREF_0	IO L019_0	IO L019_0	IO L119_0 VREF_0	IO L119_0 VREF_0	GND	VCCAUX	IO L119_0 GOLK1	GND	IO L139_0	IO L139_0	IO L139_0	IO L139_0	IO L139_0	IO L139_0	IO L139_0	IO L139_0	IO L139_0	W	
	Y	IO L449_0	IO L449_0	GND	IO L029_0 VREF_0	IO L029_0	IO L029_0	IO L029_0	IO L119_0 VREF_0	IO L119_0 VREF_0	IO L119_0 VREF_0	IO L119_0 GOLK1	IO L119_0 GOLK1	IO L119_0 GOLK1	IO L119_0	IO L119_0	IO L119_0	IO L119_0	IO L119_0	IO L119_0	IO L119_0	IO L119_0	IO L119_0	Y	
	A	IO L459_0	IO L459_0	IO L029_0	IO L049_0	VCC0_0	IO L029_0	GND	IO L129_0	VCC0_0	IO L129_0	GND	IO L119_0 GOLK1	VCC0_0	IO L129_0	IO L129_0	IO L129_0	IO L129_0	VCC0_0	IO L129_0	IO L129_0	IO L129_0	IO L129_0	A	
	A	IO L459_0	IO L459_0	IO L029_0	IO L049_0	VCC0_0	IO L029_0	GND	IO L129_0	VCC0_0	IO L129_0	GND	IO L119_0 GOLK1	VCC0_0	IO L129_0	IO L129_0	IO L129_0	IO L129_0	VCC0_0	IO L129_0	IO L129_0	IO L129_0	IO L129_0	A	
B	GND	IO L039_0	IO L049_0	IO L039_0	IO L039_0	IO L039_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	IO L109_0	B		

- 195 I/O: Unrestricted, general-purpose user I/O
- 60 INPUT: Unrestricted, general-purpose input pin
- 51 DUAL: Configuration pins, then possible user I/O
- 33 VREF: User I/O or input voltage reference for bank
- 32 CLK: User I/O, input, or clock buffer input
- 2 SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
- 2 CONFIG: Dedicated configuration pins
- 4 JTAG: Dedicated JTAG port pins
- 53 GND: Ground
- 24 VCC0: Output voltage supply for bank
- 15 VCCINT: Internal core supply voltage (+1.2V)
- 10 VCCAUX: Auxiliary supply voltage (+3.3V)
- 3 N.C.: Not connected

Progetto FPGA Spartan-3E





RS232

XC3S500E

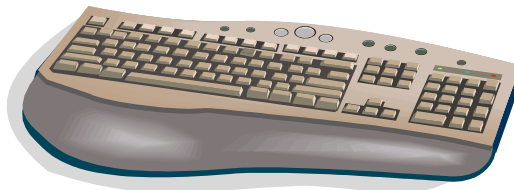
RS232 interface

ADC interface

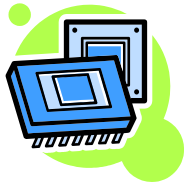
DAC interface

PS2 interface

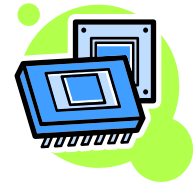
PS2



ADC



DAC



Tools

ISE: Integrated System Environment, from HDL to bitstream file

Chipscope: debug tool, watch internal signals

