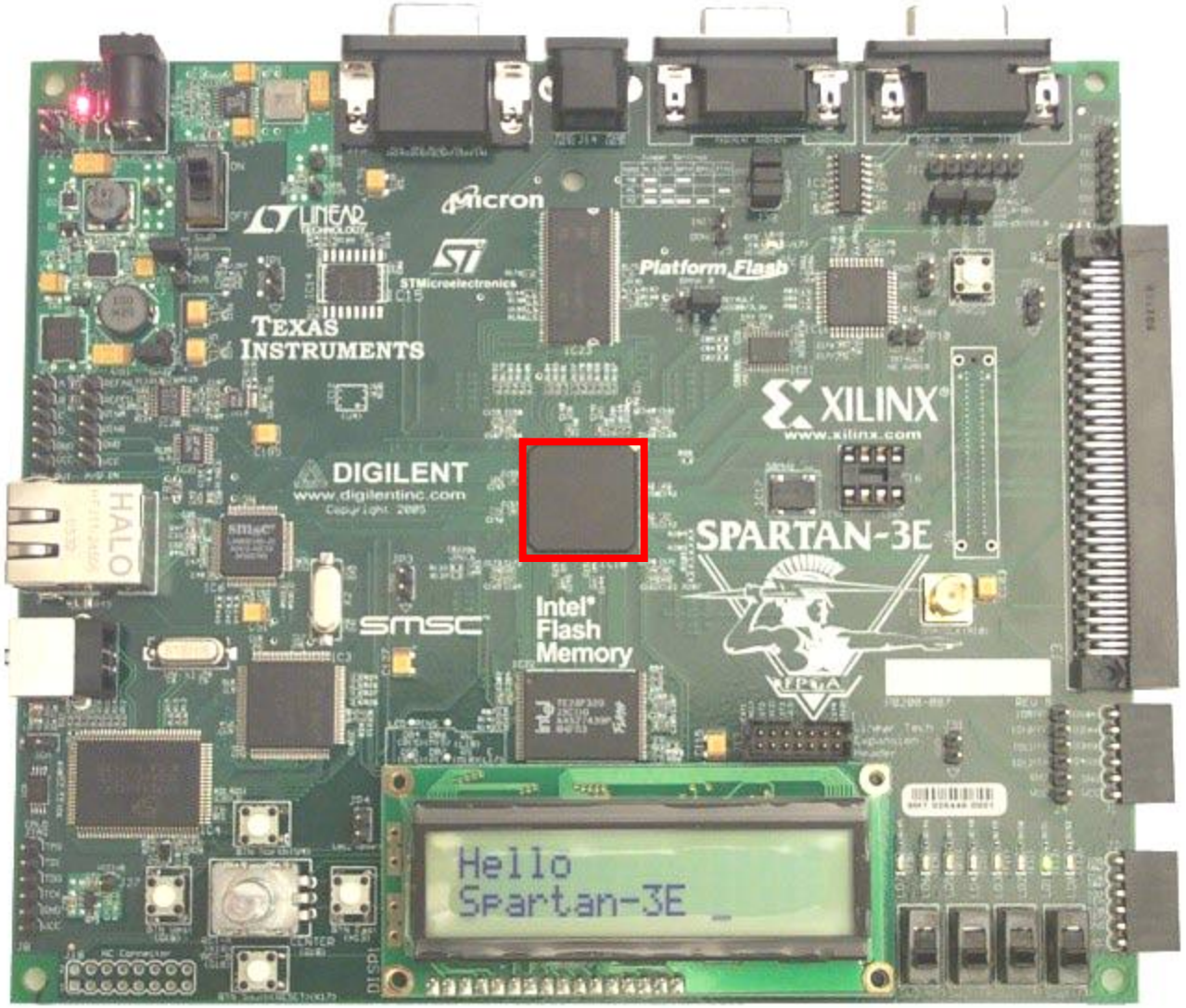
Xilinx demo board: XC3ES500E Spartan3E FPGA



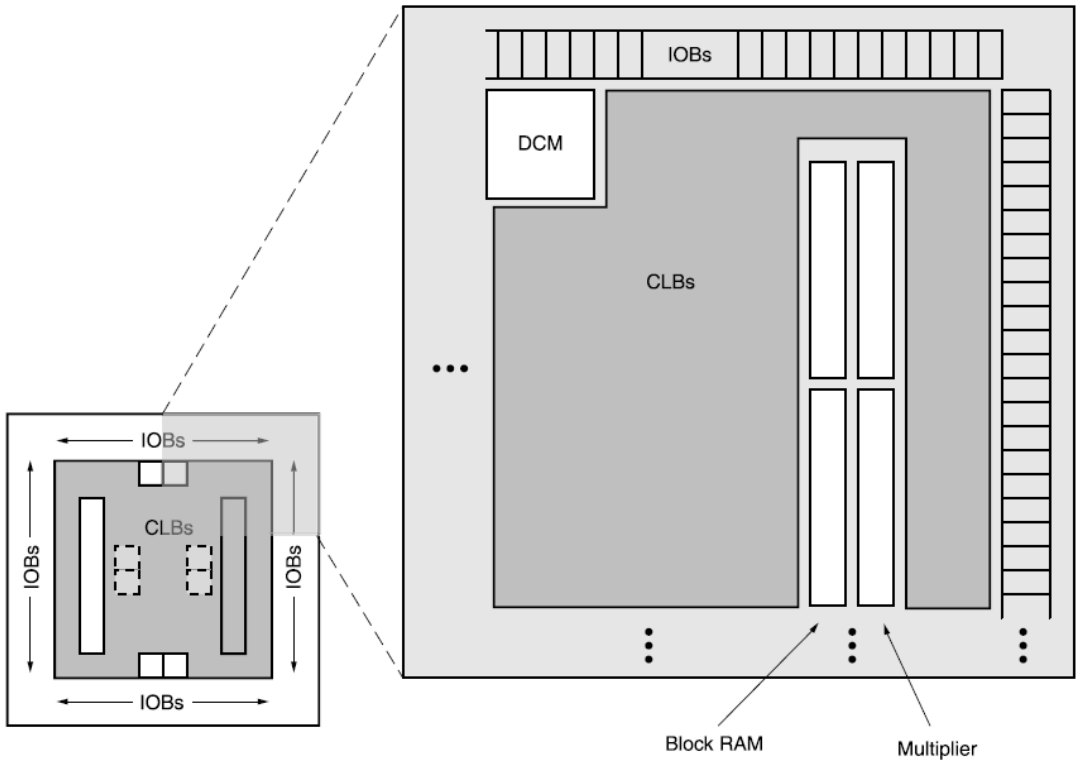
XC3ES500E Spartan3 FPGA

Table 1: **Summary of Spartan-3E FPGA Attributes**

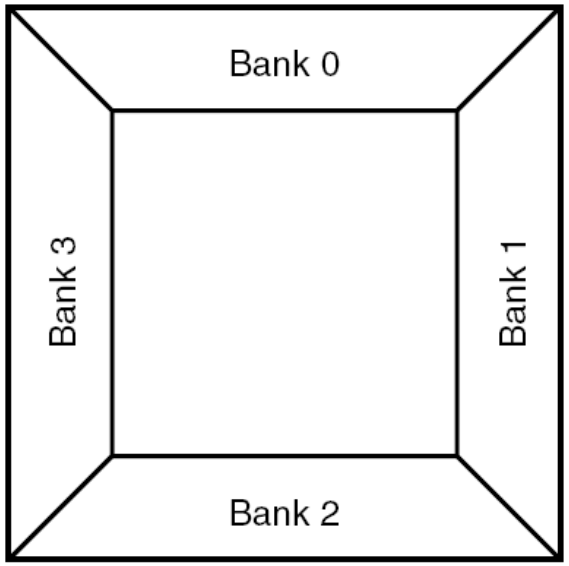
Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.



XC3ES500E pinout



I/O Capabilities

The Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

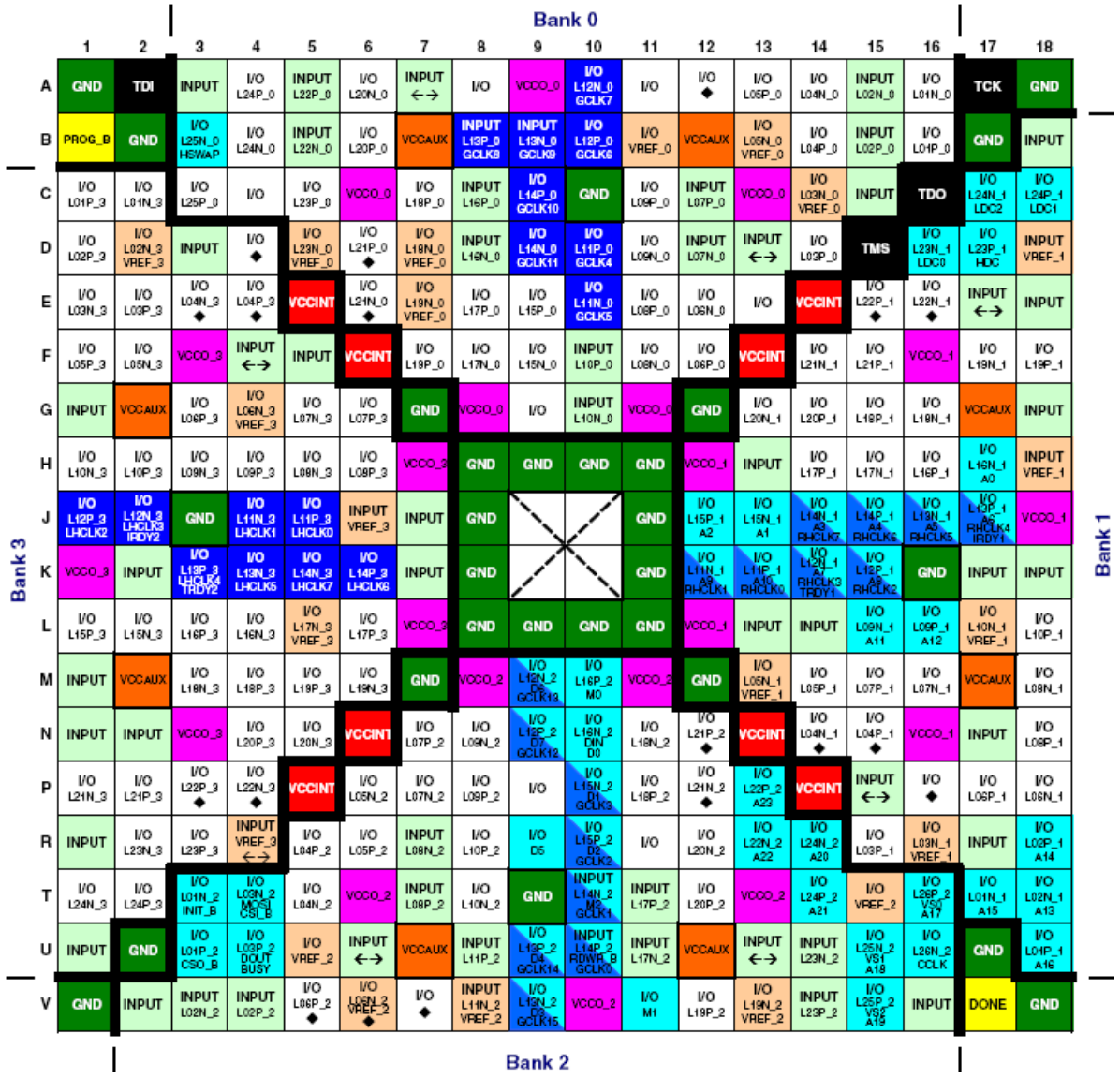
Spartan-3E FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz, and in some devices, 66 MHz
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

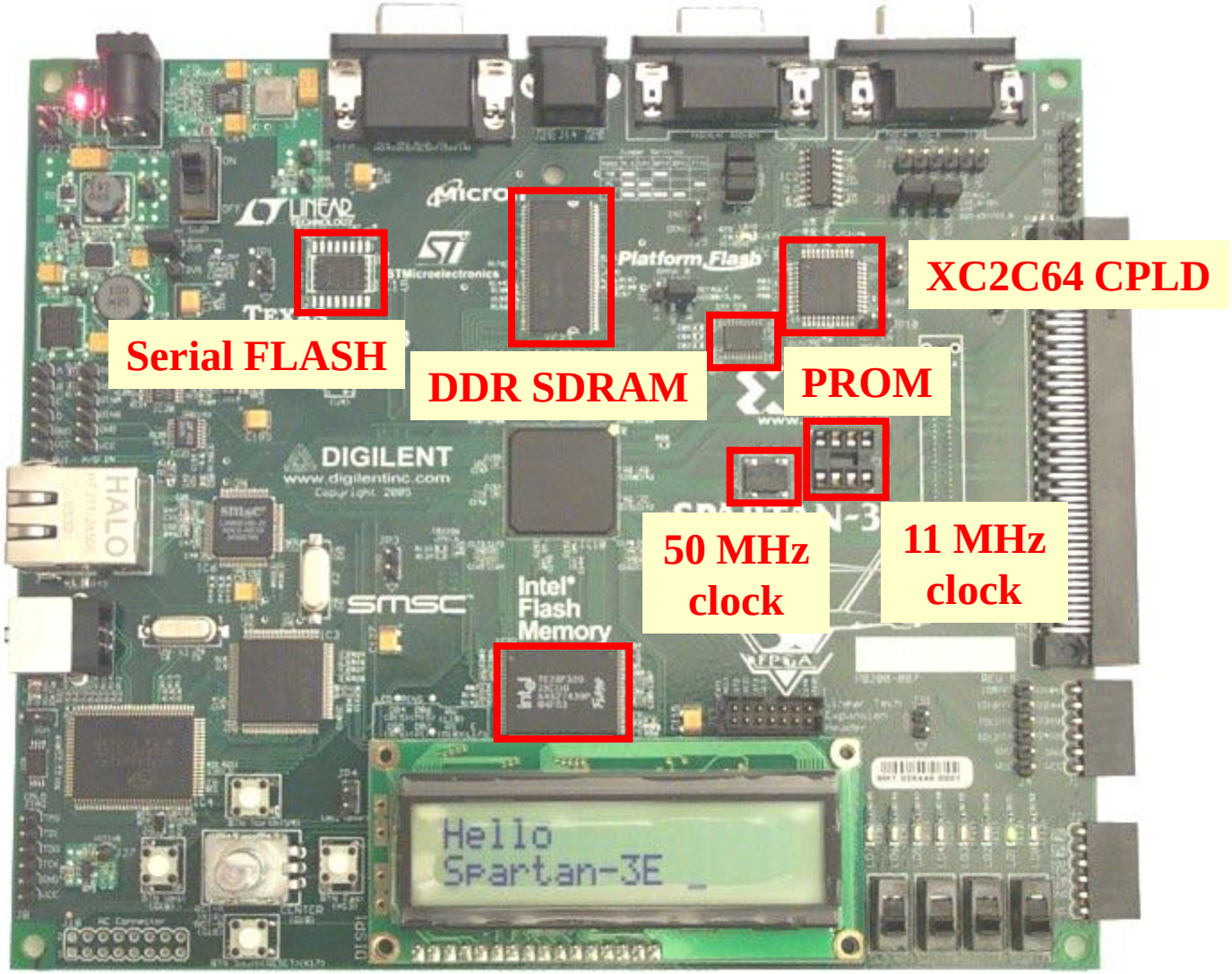
Spartan-3E FPGAs support the following differential standards:

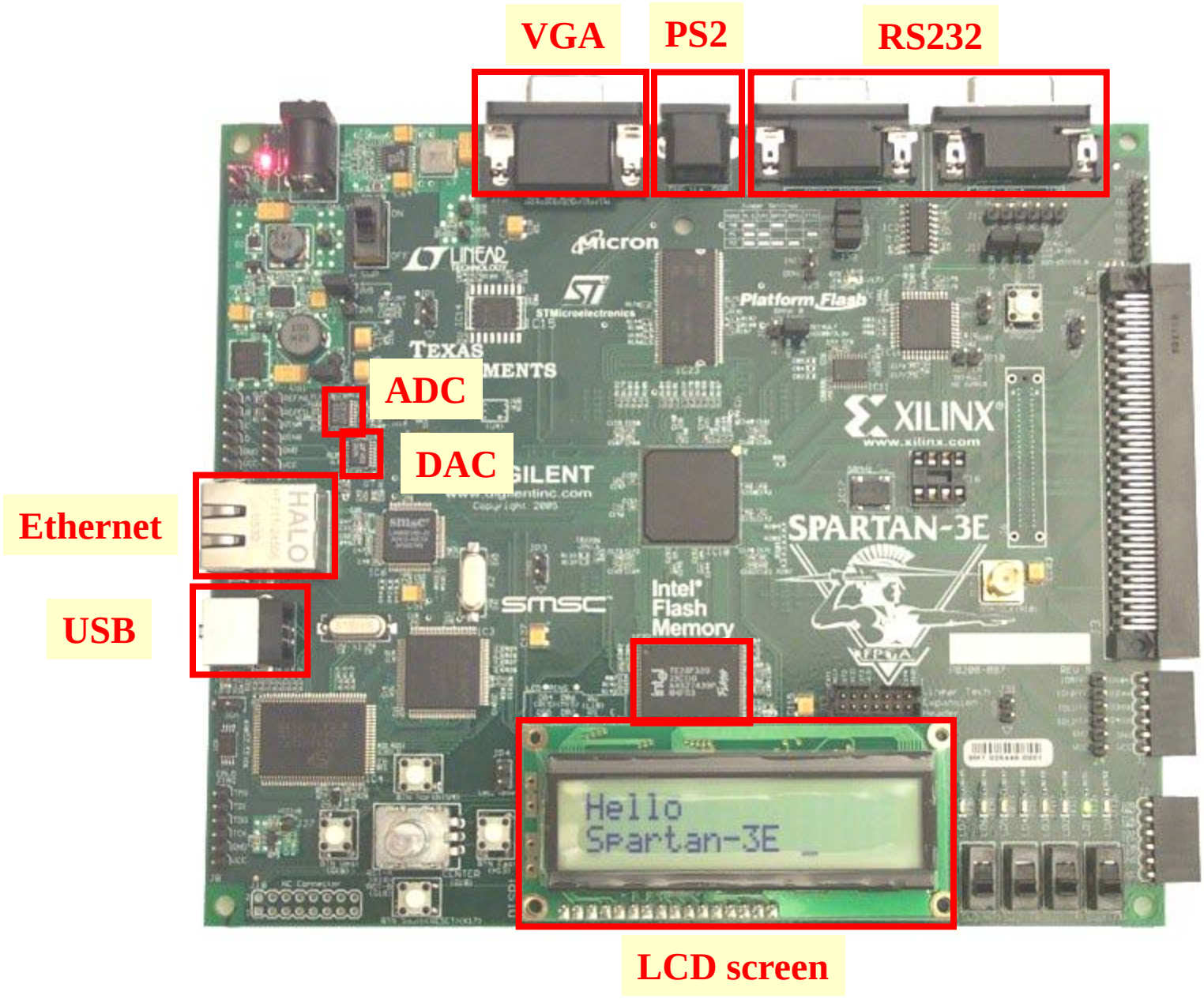
- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

XC3ES500E pinout

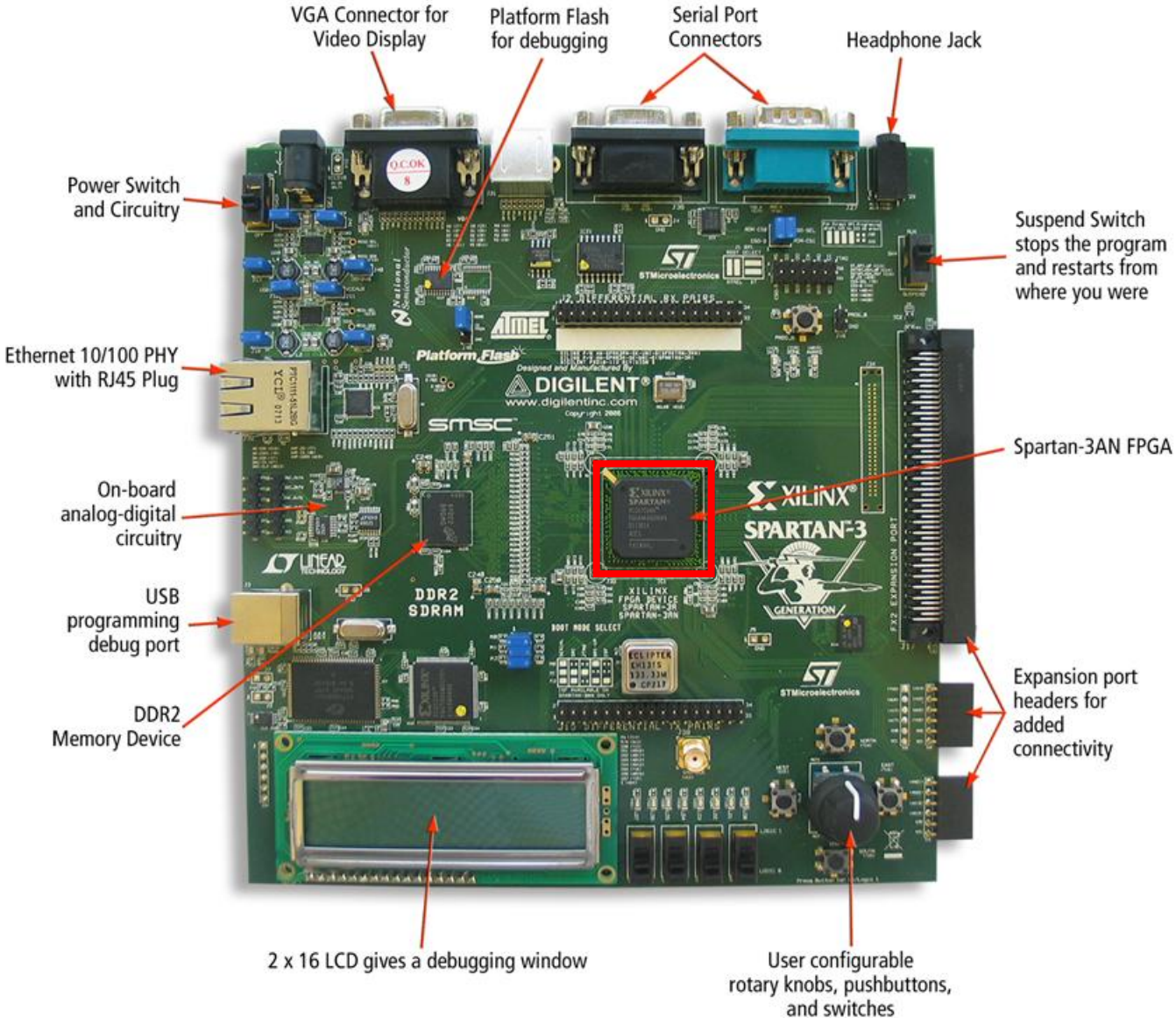


102-120	**I/O:** Unrestricted, general-purpose user I/O
47-48	**INPUT:** Unrestricted, general-purpose input pin
2	**CONFIG:** Dedicated configuration pins
18	**N.C.:** Not connected. Only the XC3S500E has these pins (◆).
46	**DUAL:** Configuration pin, then possible user-I/O
16	**CLK:** User I/O, input, or global buffer input
4	**JTAG:** Dedicated JTAG port pins
28	**GND:** Ground
20-21	**VREF:** User I/O or input voltage reference for bank
20	**VCCO:** Output voltage supply for bank
8	**VCCINT:** Internal core supply voltage (+1.2V)
8	**VCCAUX:** Auxiliary supply voltage (+2.5V)


Serial FLASH
DDR SDRAM
XC2C64 CPLD
PROM
50 MHz clock
11 MHz clock
DIGILENT
www.digilentinc.com
Intel Flash Memory
smsc
Hello
Spartan-3E

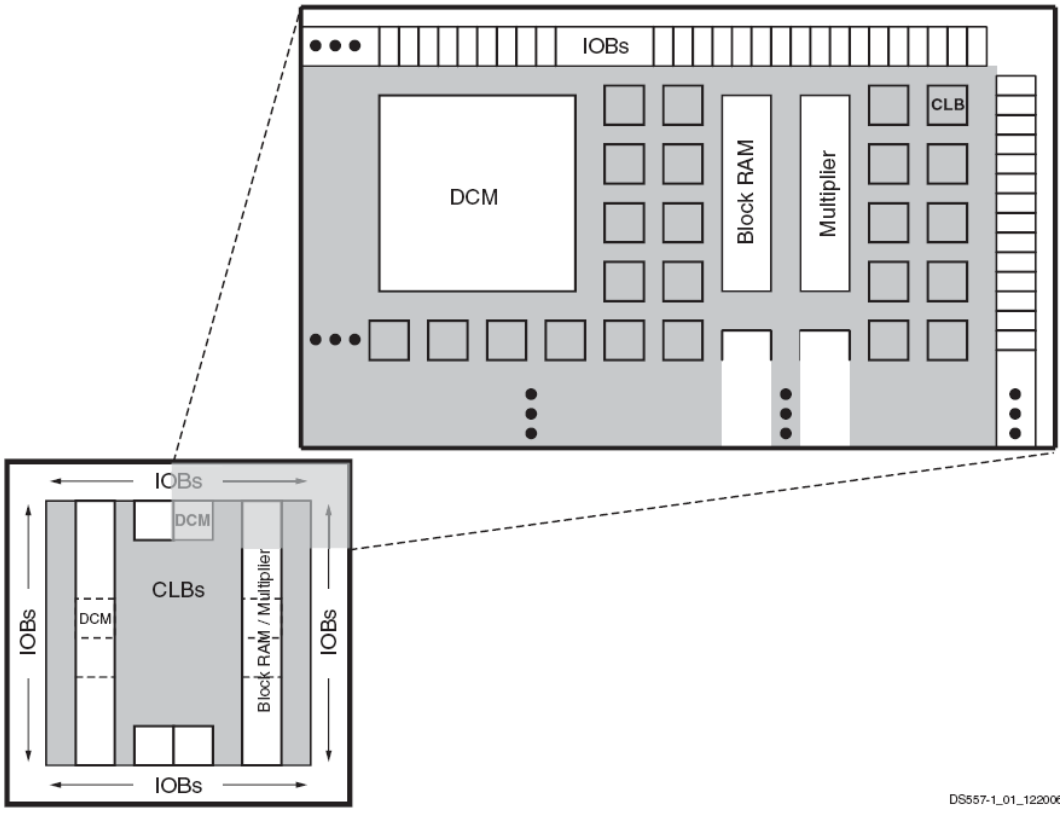

VGA
PS2
RS232
ADC
DAC
Ethernet
USB
LCD screen
Hello
Spartan-3E
XILINX
SPARTAN-3E
Micron
Platform Flash
Intel
Flash
Memory
smsc
TEXAS

Xilinx demo board: XC3ES700AN Spartan3AN FPGA

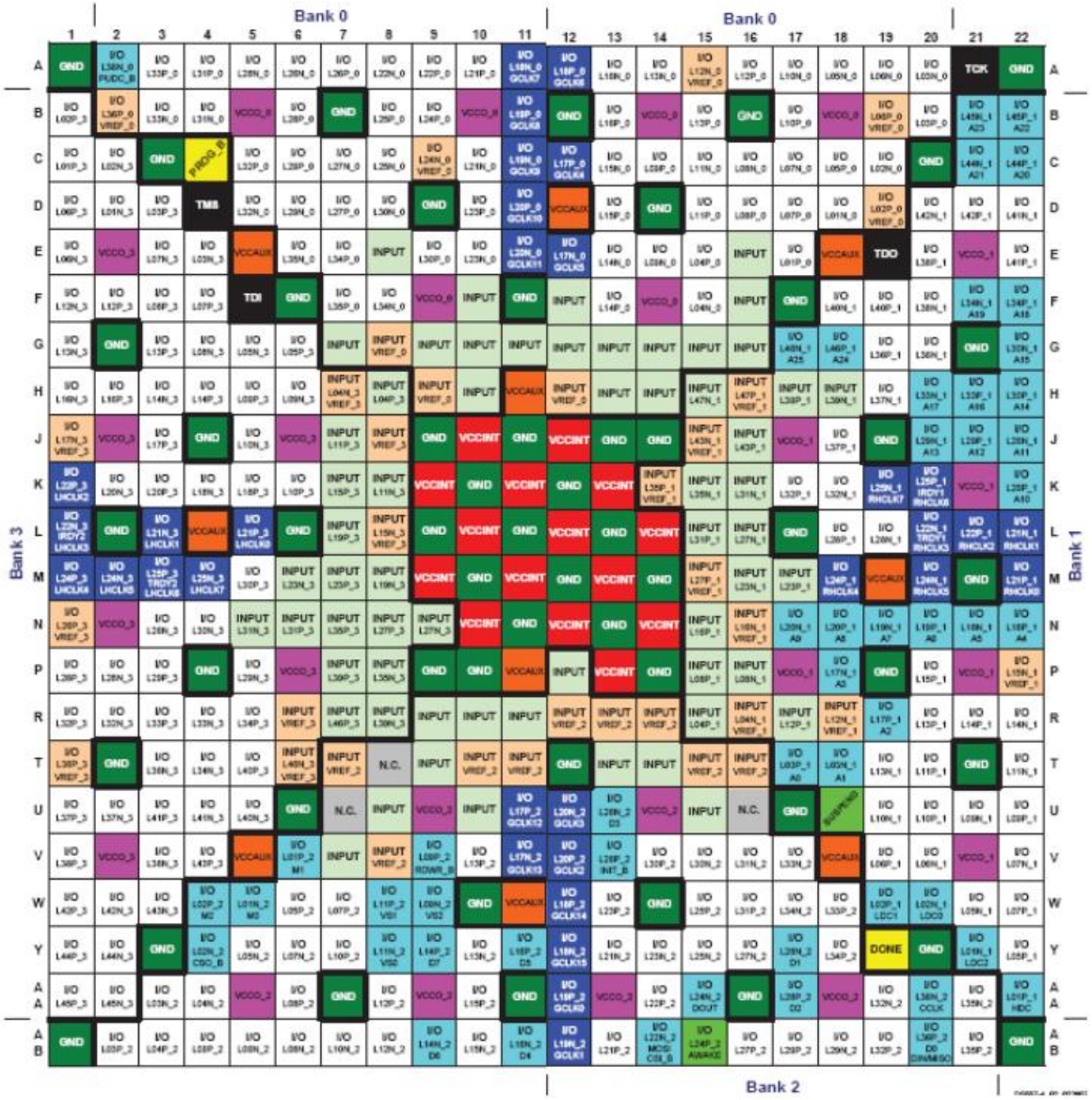


XC3ES700AN Spartan3 FPGA

Device	System Gates	Equivalent Logic Cells	CLBs	Slices	Distributed RAM Bits(1)	Block RAM Bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs	Bitstream Size (1)	In-System Flash Bits
XC3S50AN	50K	1,584	176	704	11K	54K	3	2	108	50	427K	1M
XC3S200AN	200K	4,032	448	1792	28K	288K	16	4	195	90	1,168K	4M
XC3S400AN	400K	8,064	896	3,584	56K	360K	20	4	311	142	1,842K	4M
XC3S700AN	700K	13,248	1472	5,888	92K	360K	20	8	372	165	2,669K	8M
XC3S1400AN	1400K	25,344	2816	11,264	176K	576K	32	8	502	227	4,644K	16M

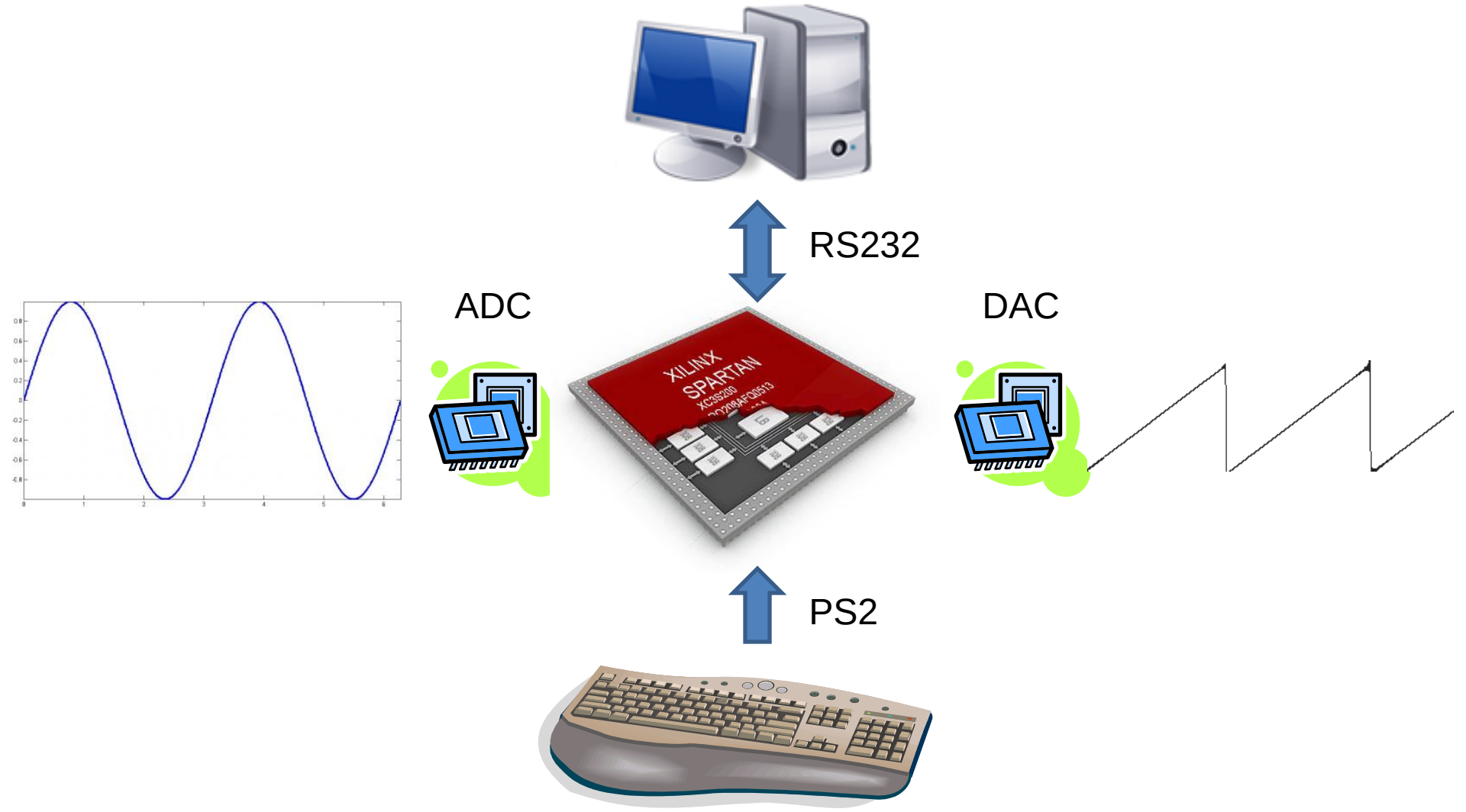


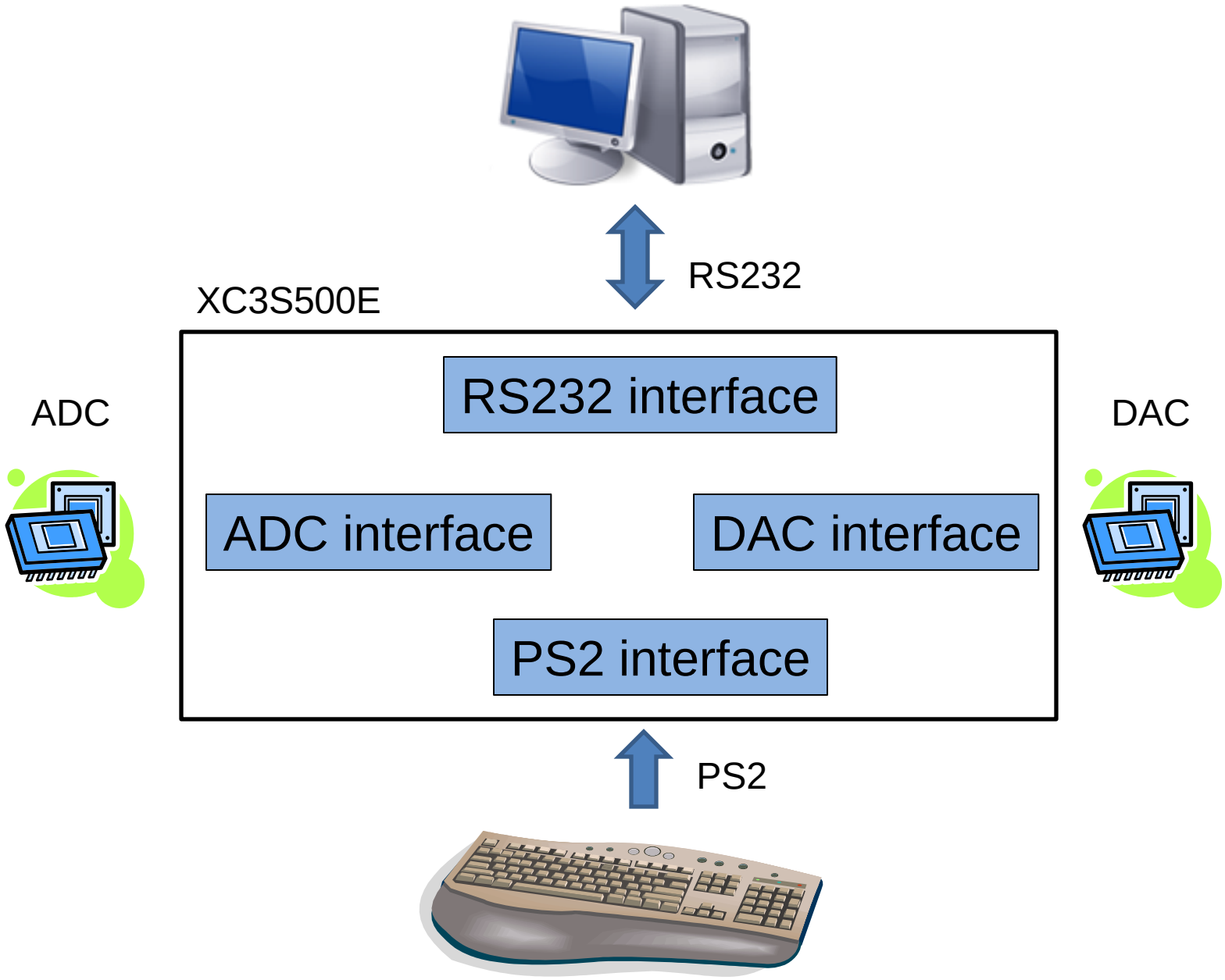
XC3S700AN-4FGG484C



195	**I/O:** Unrestricted, general-purpose user I/O
60	**INPUT:** Unrestricted, general-purpose input pin
51	**DUAL:** Configuration pins, then possible user I/O
33	**VREF:** User I/O or input voltage reference for bank
32	**CLK:** User I/O, input, or clock buffer input
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
2	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
53	**GND:** Ground
24	**VCCO:** Output voltage supply for bank
15	**VCCINT:** Internal core supply voltage (+1.2V)
10	**VCCAUX:** Auxiliary supply voltage (+3.3V)
3	**N.C.:** Not connected

Progetto FPGA Spartan-3E




RS232
XC3S500E
ADC
RS232 interface
DAC
ADC interface
DAC interface
PS2 interface
PS2

Tools

ISE: Integrated System Environment, from HDL to bitstream file

Chipscope: debug tool, watch internal signals