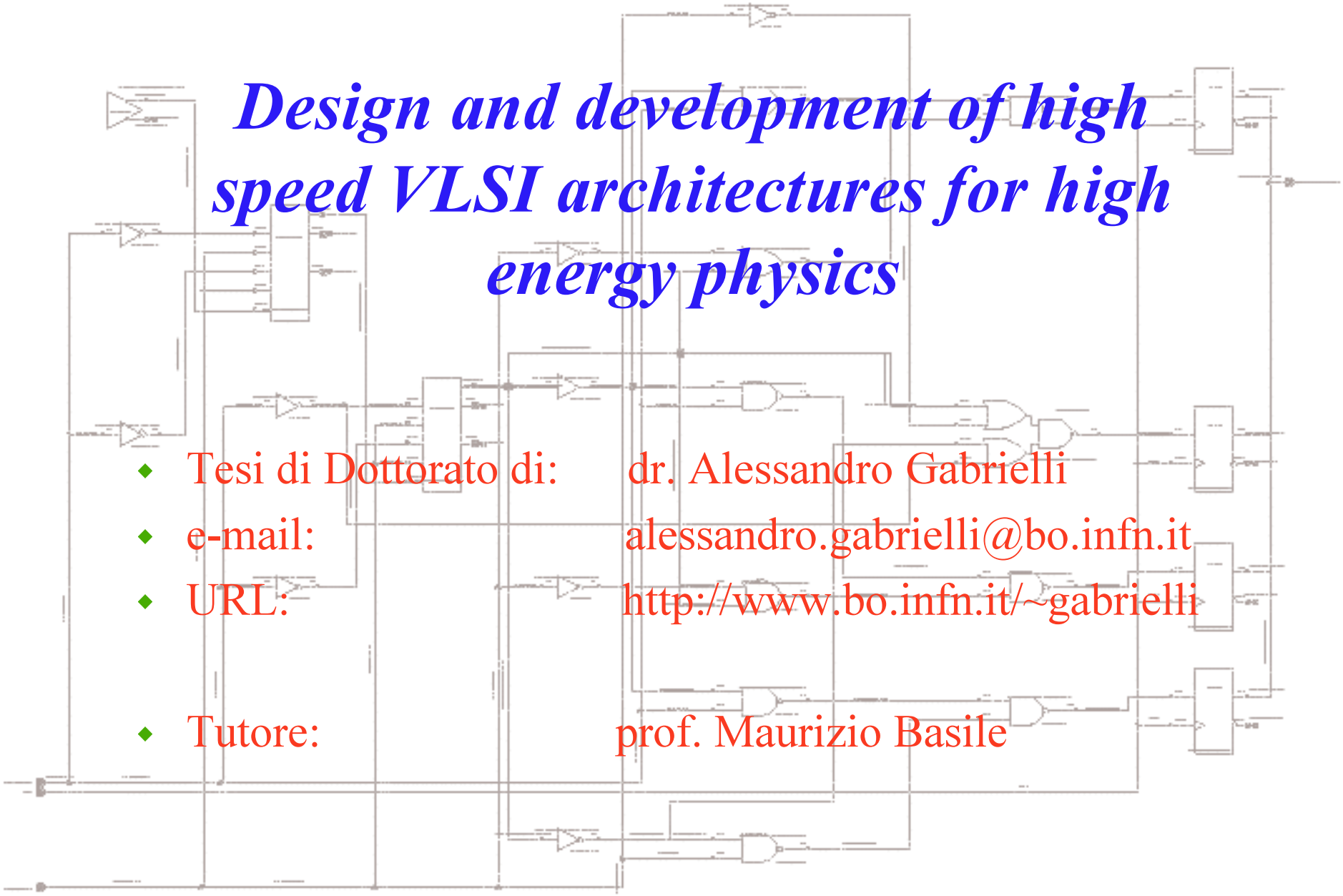
Design and development of high speed VLSI architectures for high energy physics



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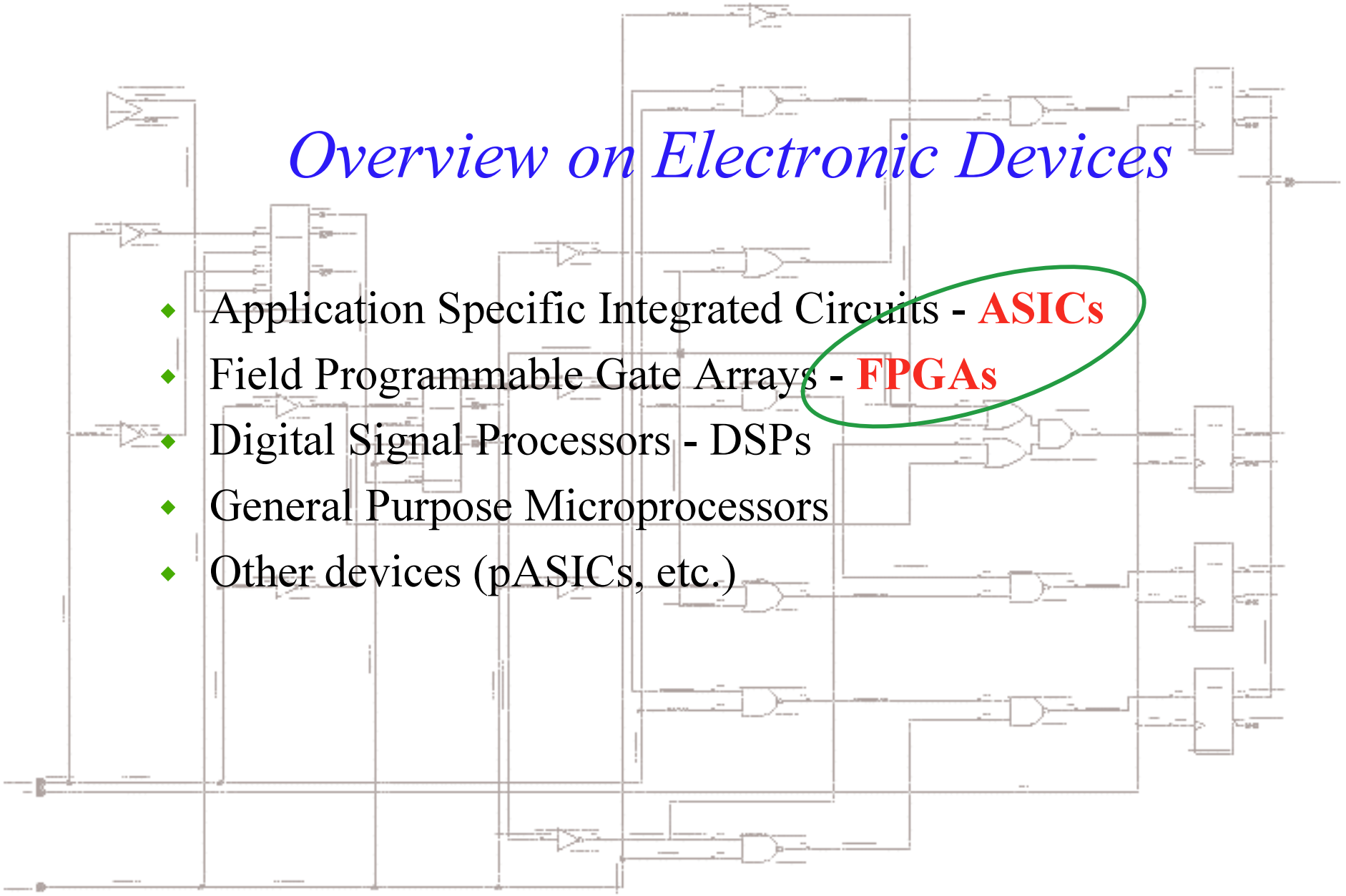
- e-mail: alessandro.gabrielli@bo.infn.it
- URL: http://www.bo.infn.it/~gabrielli

- Tutore: prof. Maurizio Basile

Talk Presentation

- Overview on Electronic Devices
- Pipeline Architecture: Example (5 slides)
- The Problem of Triggering in High Energy Physics (2 slides)
- A Typical Digital Design Flow
- The 4-Input Fuzzy Processor (4 slides)
- Silicon Drift Electronics For ALICE ITS (5 slides)
- Control Electronics for NEMO (2 slides)

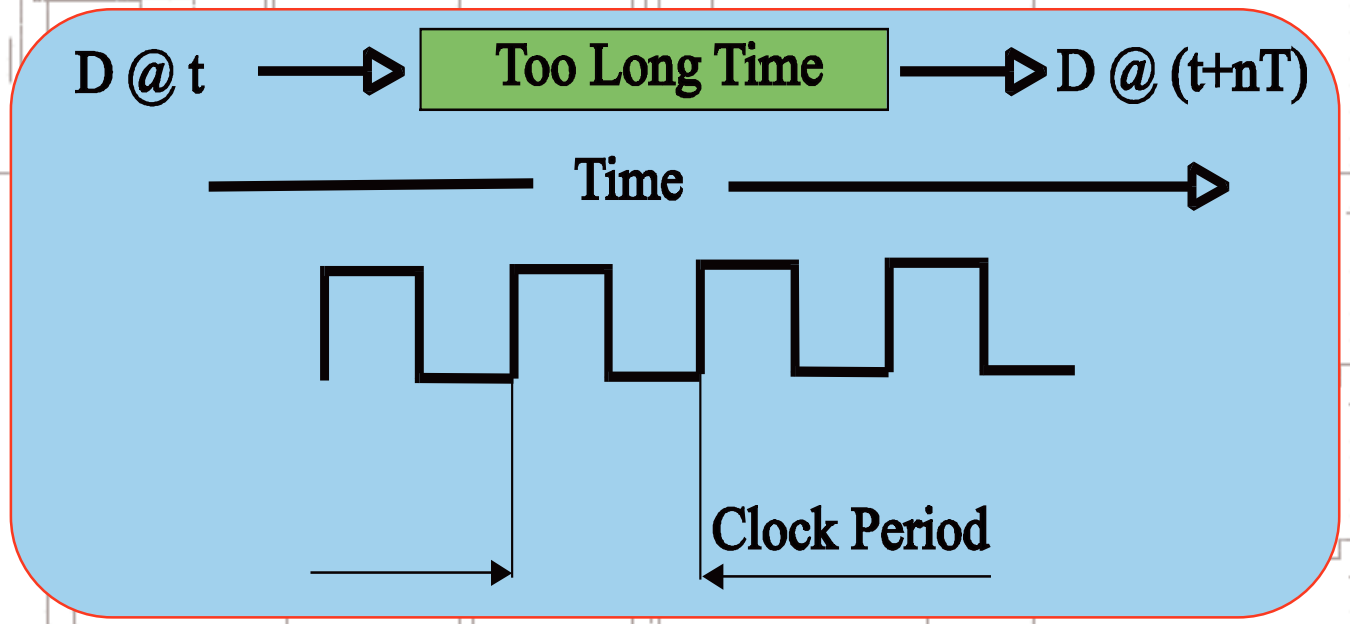
Overview on Electronic Devices



- Application Specific Integrated Circuits - **ASICs**
- Field Programmable Gate Arrays - **FPGAs**
- Digital Signal Processors - DSPs
- General Purpose Microprocessors
- Other devices (pASICs, etc.)

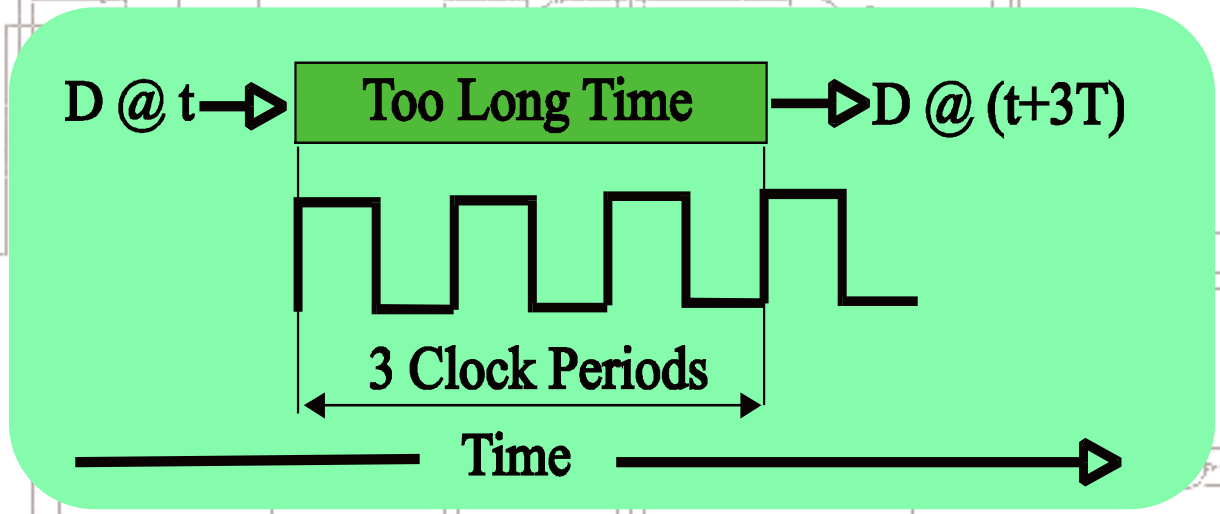
Pipeline Architecture

Suppose a given task takes a long time compared to the clock period



Pipeline Architecture

or e ample the task takes clock periods

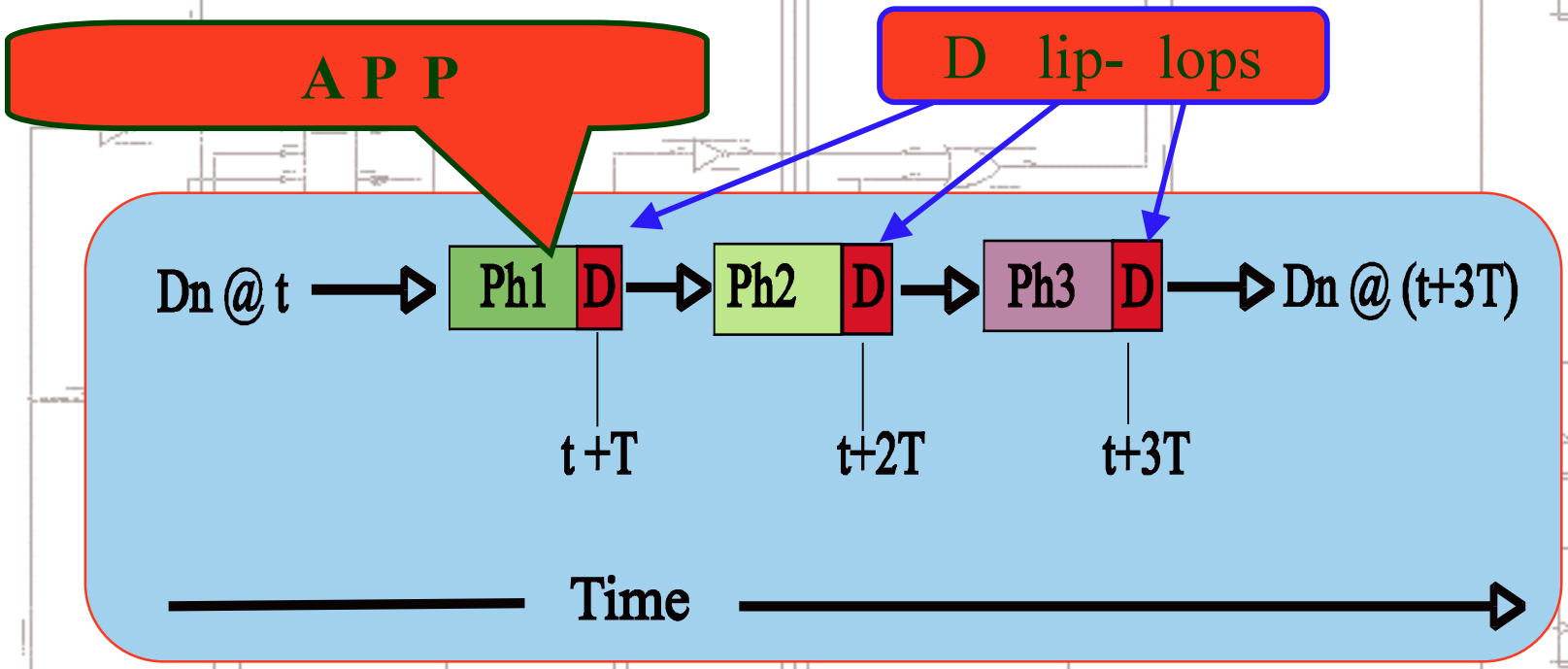


I data must e processed the s stem takes

P ithout using

a **P P** architecture

Pipeline Architecture

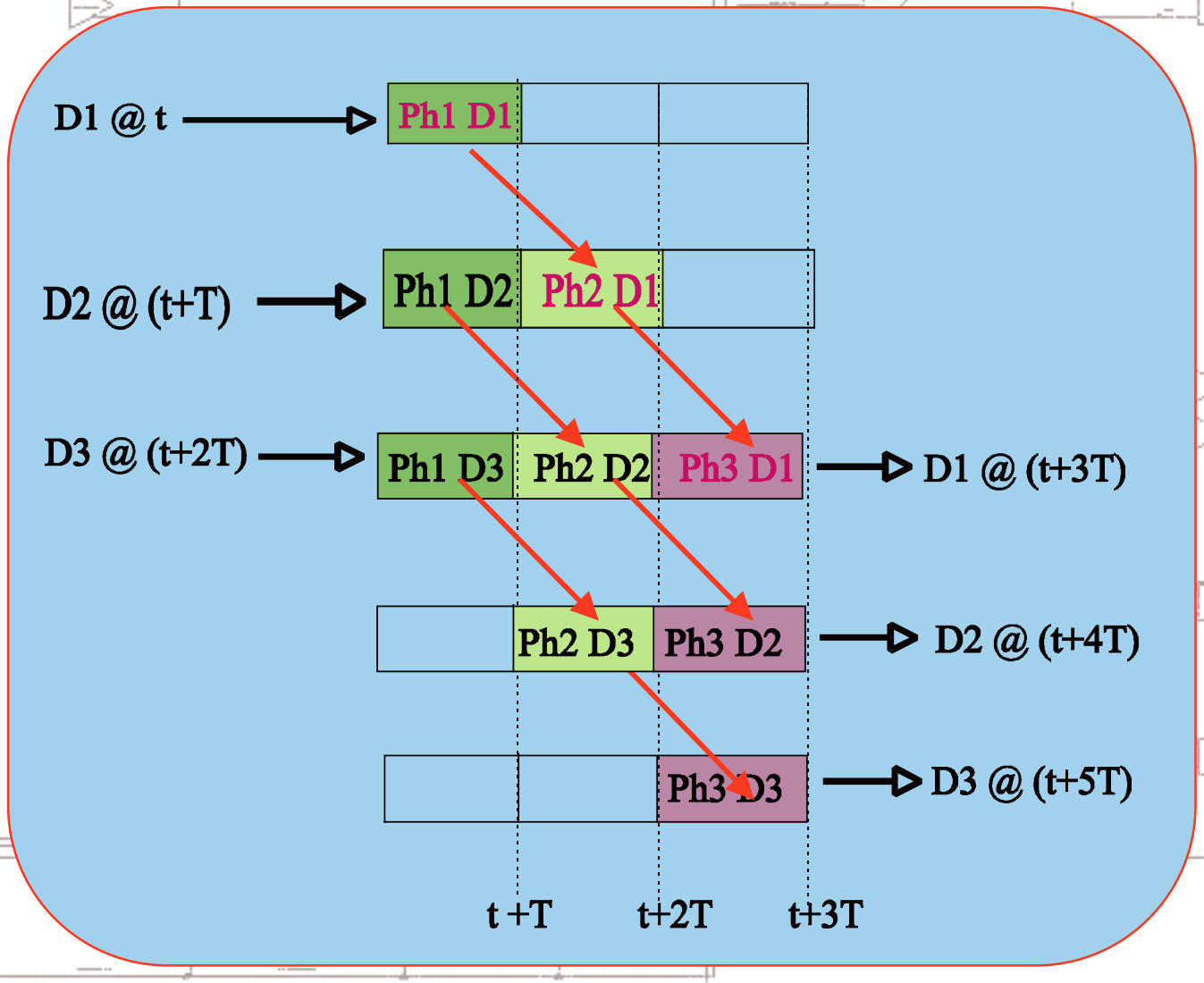


Suppose the task is divided into

P P P A carried out at

the same time on di erent data

Pipeline Architecture



he

P P

architecture

takes

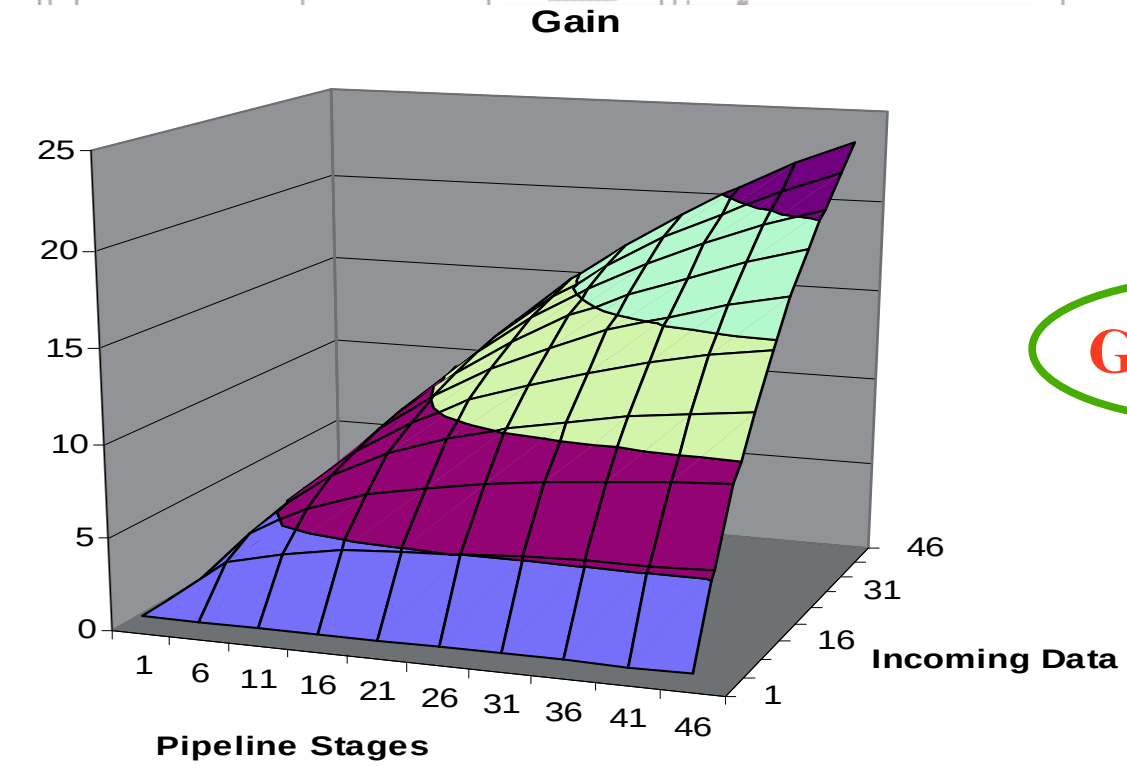
P or

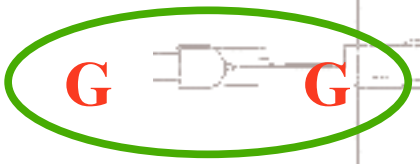
carr ing out

the same task

Pipeline Architecture

ith data, **P** ( ) pipeline phases, the pipeline architecture takes **G P** clock periods instead o **P** periods o a non pipeline one



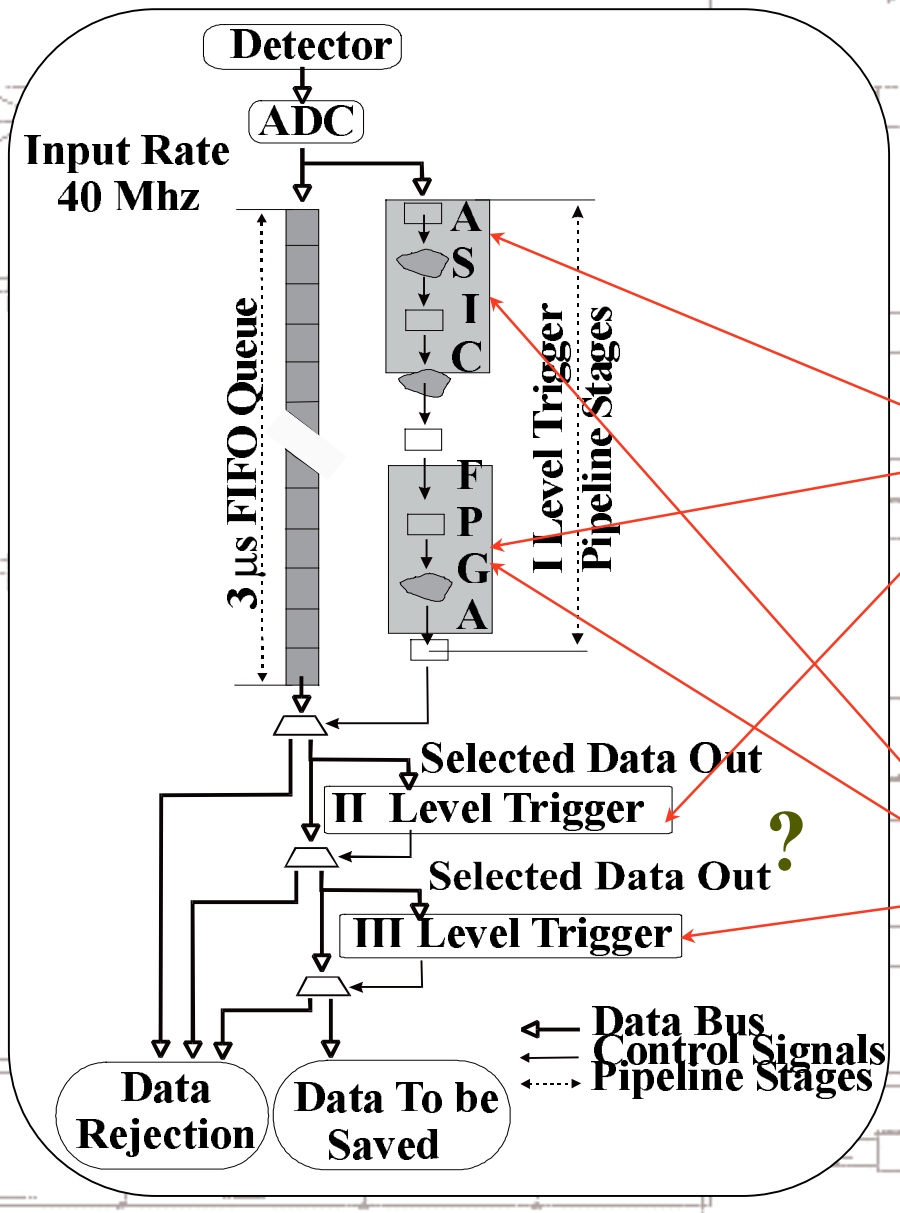


he Pr le ri erin in i h ner Ph ic

G A

- Input ates (M in C)
- rigger evel (I - II - III)
- echnolog (Digital-Analog, CMOS- iCMOS-GaAs)
- ASIC - PGA
- adiation olerant - adiation ard
- Po er Consumption

The Problem of Triggering in High Energy Physics

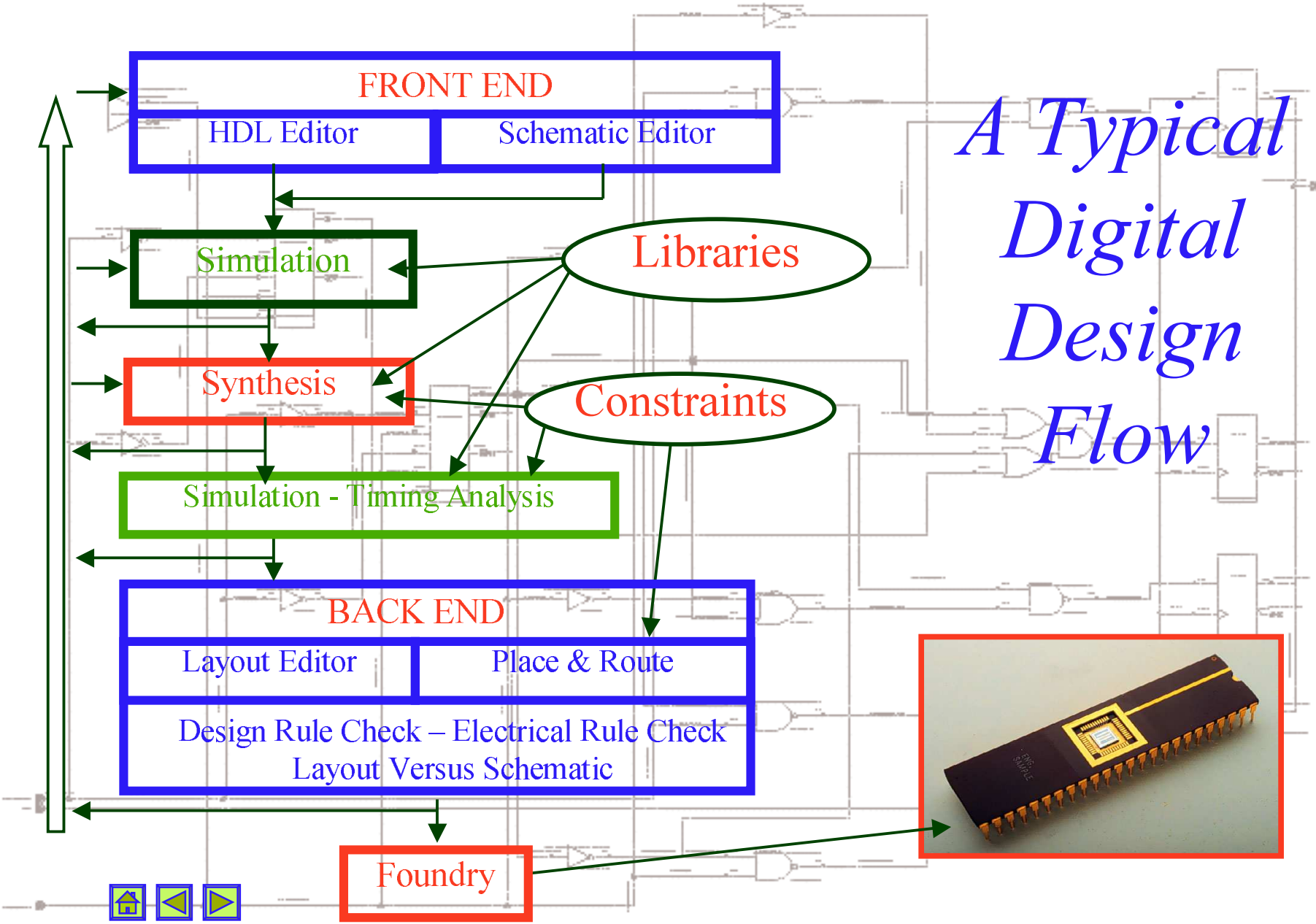


ASIC - Fuzzy Processor

FPGA - Programmable Device

13

A Typical Digital Design Flow



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The 4-Input Fuzzy Processor

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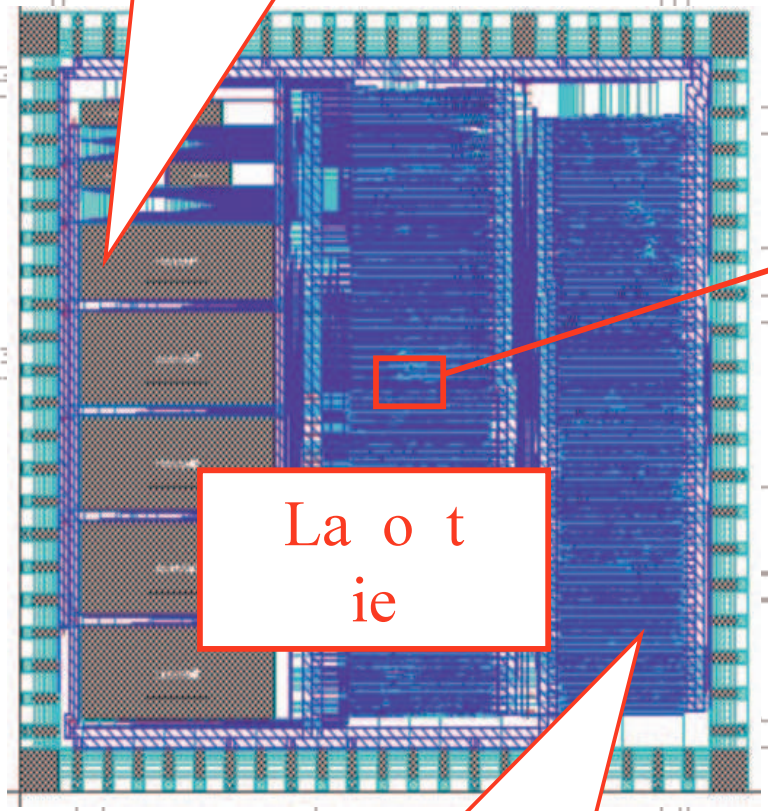

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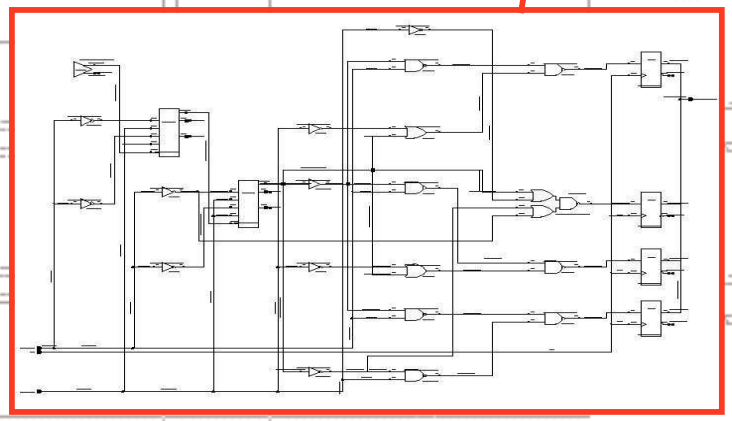

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HW: SUN Sparc5

SW:Cadence 94.01

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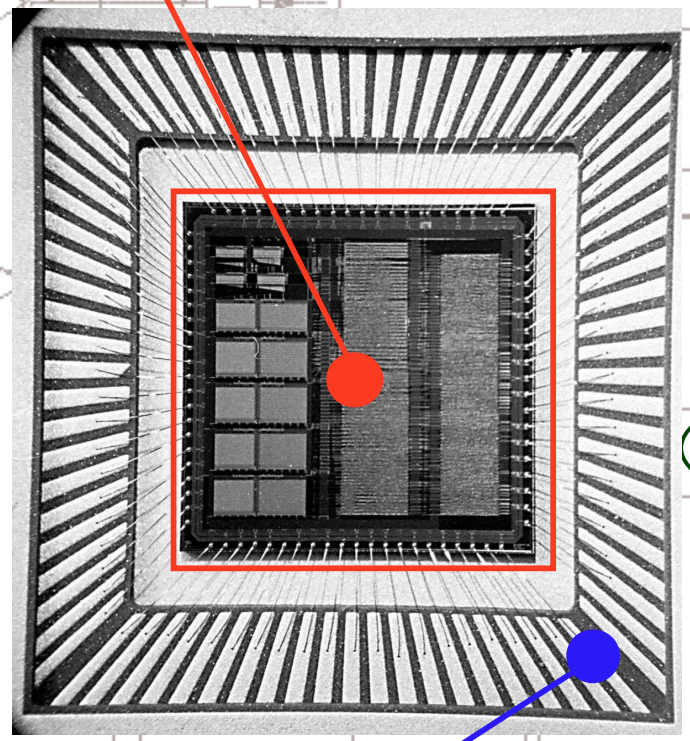
The 4-Input Fuzzy Processor



- Four 7-bit 7-Fuzzy-Set Inputs
- One 7-bit 128-Fuzzy-Set Output
- 2401 Fuzzy Rules
- 4 → 16 Active Rule
- 80 → 320 ns I/O Delay
- 50 MHz
- ES2 0.7 µm D DMSP
- 1300 mW @ 50 MHz

Digital
Double Metal
Singol Poly

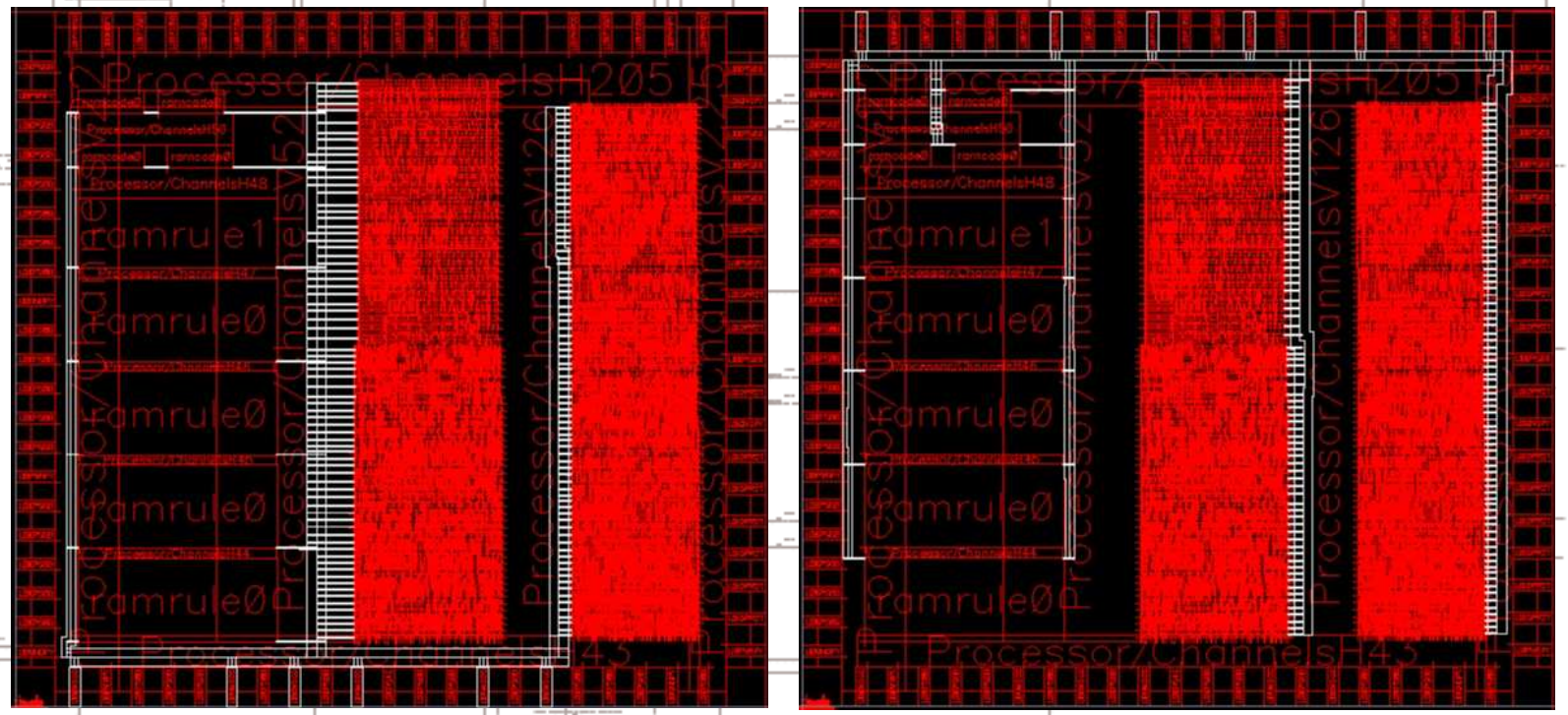
INFN
GR. 5

The 4-Input Fuzzy Processor

POWER GROUND

interdigitized 200 µm wide wires

ES2 digital 0.7µm



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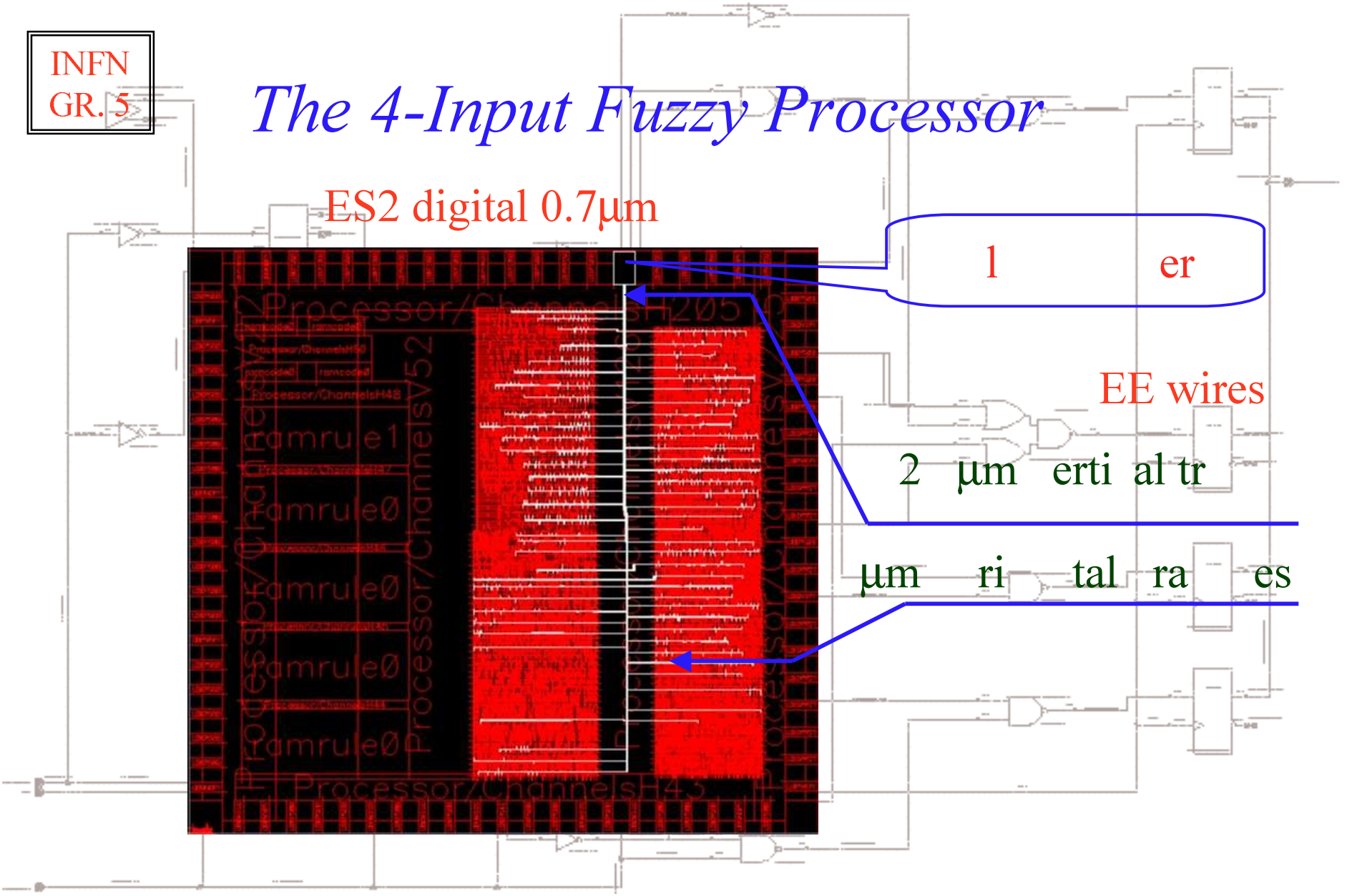
The 4-Input Fuzzy Processor

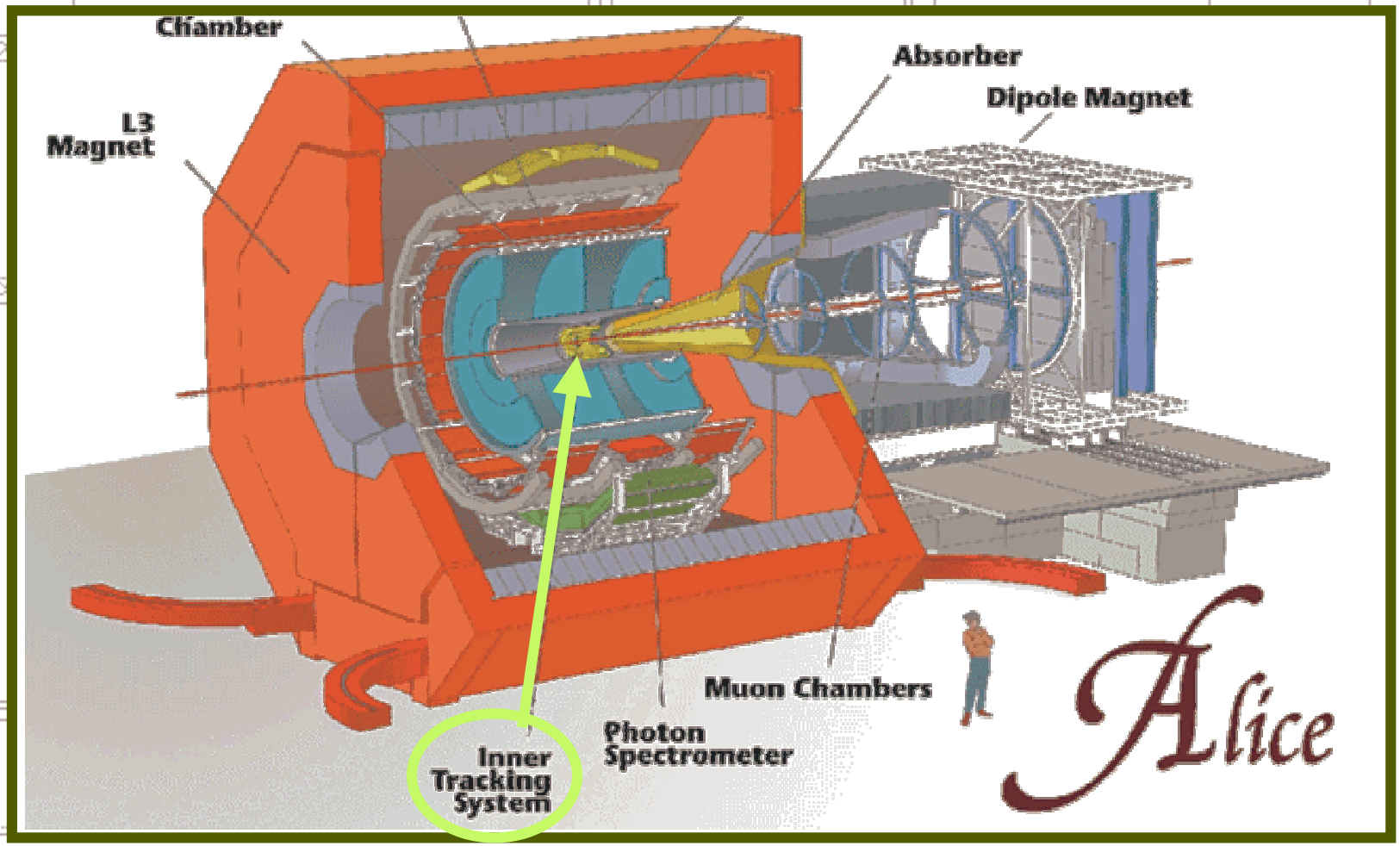
ES2 digital 0.7µm



INFN
GR. 3

Silicon Drift Electronics For ALICE ITS

(picture taken from TDR 4 June 99)



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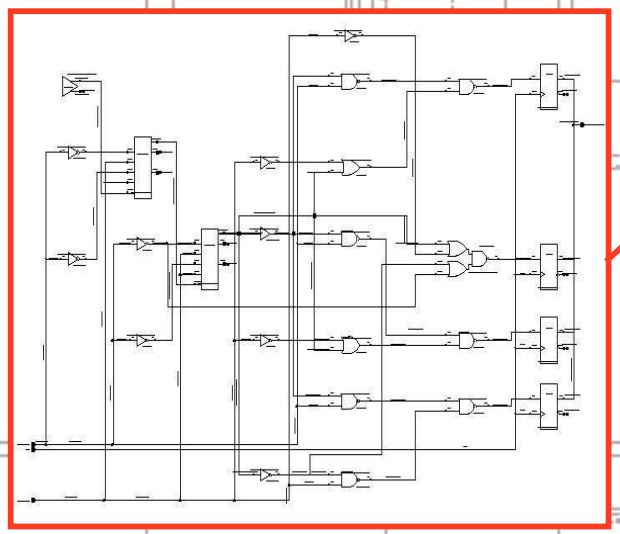
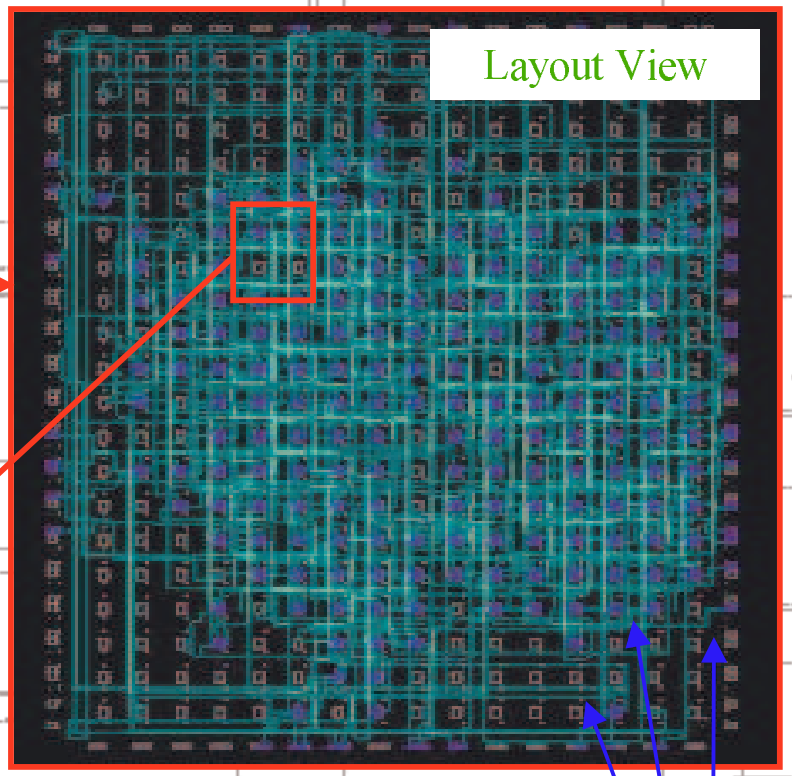
GR. 3

Silicon Drift Electronics For ALICE ITS

Electronics for the Silicon Drift Detector Data Acquisition System





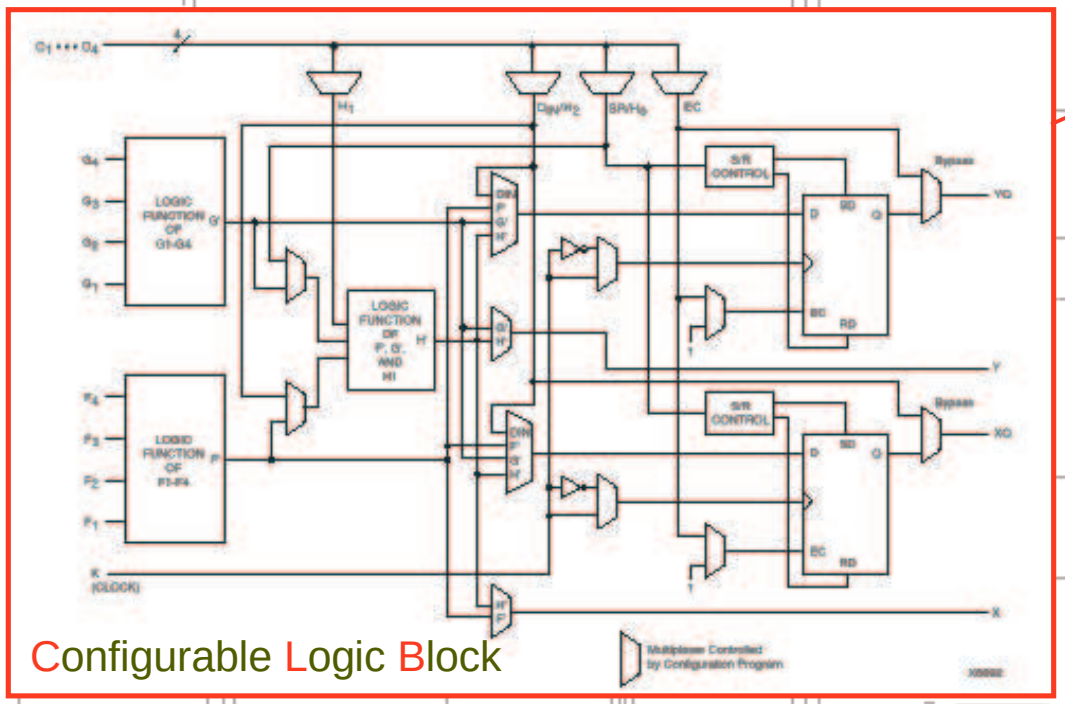
HW: SUN Sparc5 PC Pentium III

SW:Synopsys 98.08 Alliance 1.5i

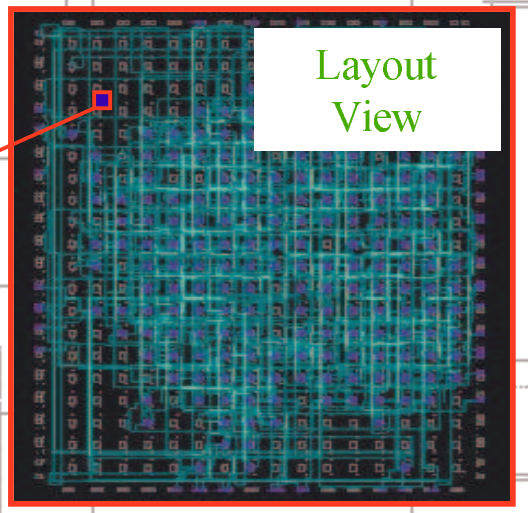
CLB

INFN GR. 3

Silicon Drift Electronics For ALICE ITS



Configurable Logic Block



Layout View

XILINX XC4000E

- ✓ high routing capacity
- ✓ system clock rates of up to 80 MHz
- ✓ internal performance over 150 MHz
- ✓ 16x1 Dual Port / 16x2 Single Port RAM
- ✓ function generators

Device	Logic Gates	RAM Bits	Typical Gate Range	CLB Matrix	Total CLBs	FlipFlops	User I/O
XC4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	256

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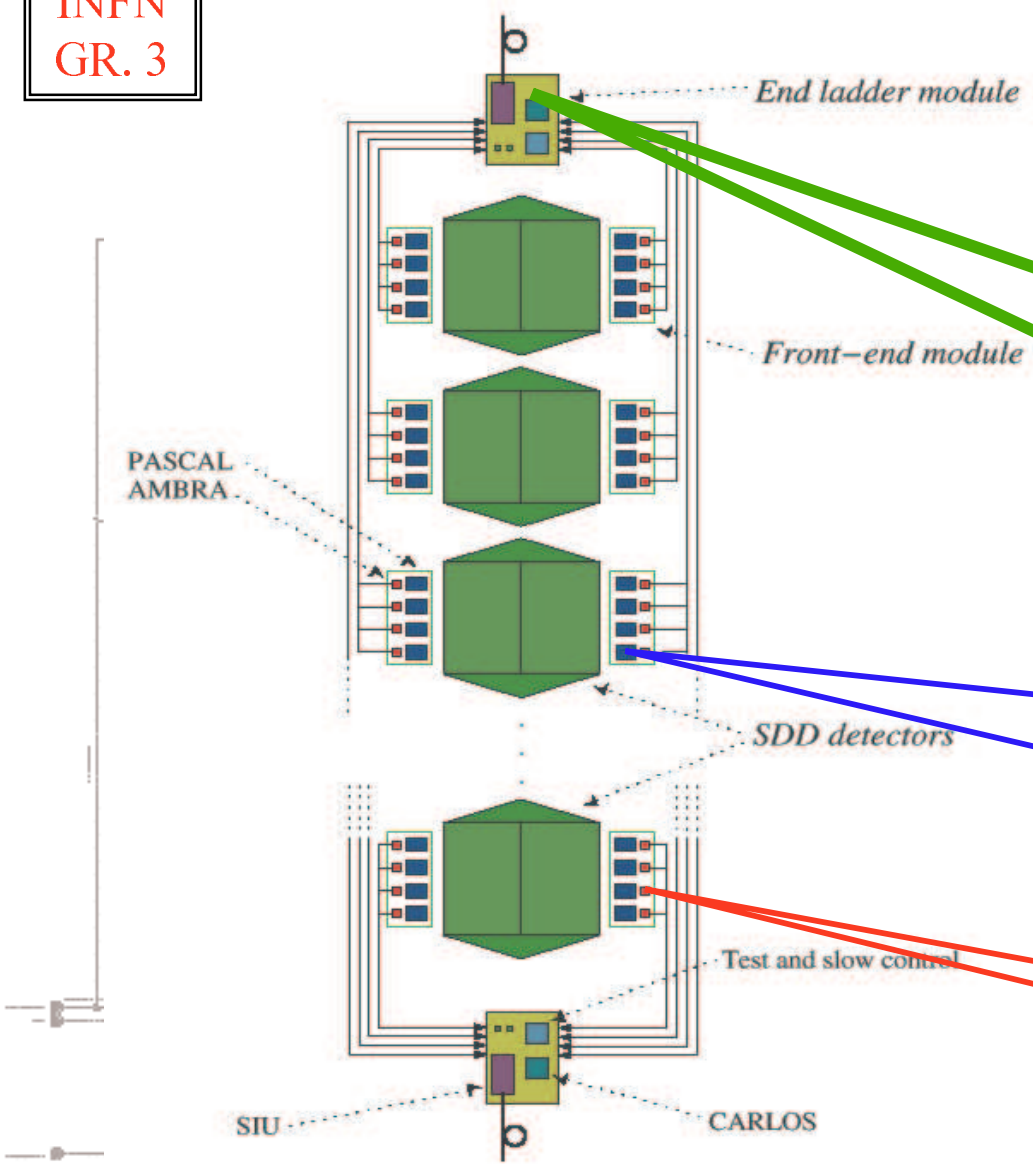
GR. 3

(picture taken from TDR 4 June 99)



Silicon Drift Electronics For ALICE ITS

Data Compression &

Packing to Optical Fiber

Preamplifier

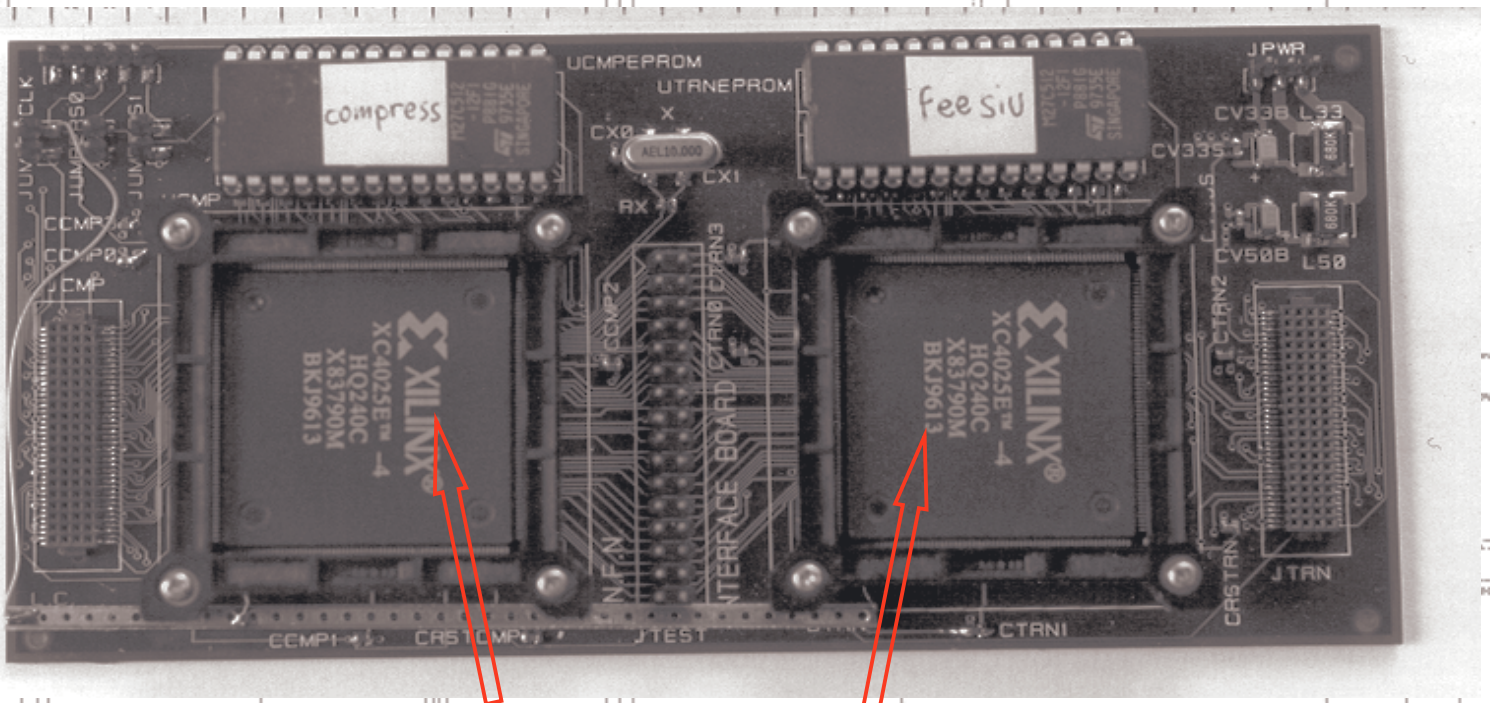
Analog Memory - ADC

Double Event Buffer

INFN
GR. 3

Silicon Drift Electronics For ALICE ITS

(picture taken from TDR 4 June 99)



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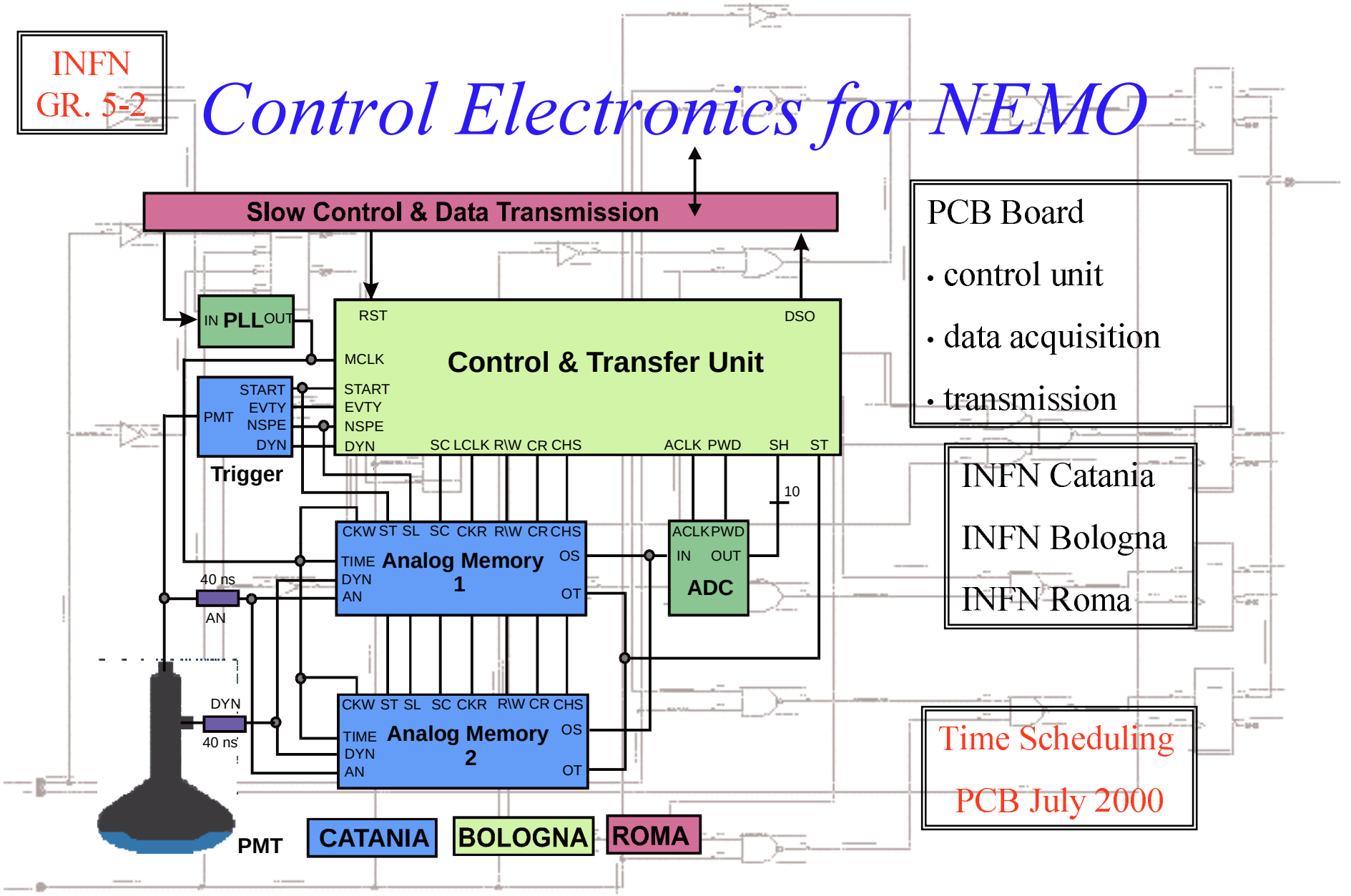
Time Scheduling

ASIC May 2000

INFN
GR. 5-2

Control Electronics for NEMO



PCB Board

- control unit
- data acquisition
- transmission

INFN Catania

INFN Bologna

INFN Roma

Time Scheduling

PCB July 2000

INFN
GR. 5-2

Control Electronics for NEMO